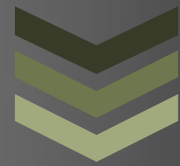


# PINE TRAINING ACADEMY



## Course Module

Summer Training on ASIC Layout and Design

### Address

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Pine Training Academy

8/15/2016

<b>ASIC Design (Analog LAYOUT)</b>		
<b>Main Module</b>	<b>FPGA LOGIC System Design using Verilog</b>	<b>Duration</b>
<b>Module -1</b> Digital System Design.	<ul style="list-style-type: none"> <li>❖ Digital System Design:-               <ul style="list-style-type: none"> <li>• Introduction to Digital System.                   <ul style="list-style-type: none"> <li>○ Number System</li> <li>○ Digital Logic Levels</li> </ul> </li> <li>• Digital Logic Circuits.                   <ul style="list-style-type: none"> <li>○ Combinational Logic Circuit.</li> <li>○ Sequential Logic Circuit.</li> </ul> </li> <li>•</li> </ul> </li> </ul>	Week-1 Month 1
<b>Module – 2</b> UNIX	<ul style="list-style-type: none"> <li>❖ UNIX               <ul style="list-style-type: none"> <li>• Basic of UNIX, how different from Windows.</li> <li>• Introduction of SHELL.</li> <li>• File and Directories.</li> <li>• Home Directories Introduction and .cshrc file formation.</li> <li>• Basic Commands-cp,mv,rm,touch,which, mkdir,cat</li> <li>• UNIX sed , cut ,awk,grep (regex),tr commands.</li> <li>• BASH shell scripting, usage of loops, arguments, array.</li> </ul> </li> </ul>	Week 2 Month 1
<b>Module -3</b> Schematic Design	<ul style="list-style-type: none"> <li>❖ BASIC COMPONENTS AND OHM’S LAW               <ul style="list-style-type: none"> <li>• Resistance</li> <li>• Capacitance</li> <li>• Inductor</li> <li>• Series Combinations</li> <li>• Parallel Combinations</li> <li>• KVL/KCL</li> <li>• Introduction to Filters</li> <li>• Low Pass Filters (Passive)</li> <li>• High Pass Filters (Passive)</li> </ul> </li> <li>❖ PHYSICS OF SEMICONDUCTORS AND DIODE CIRCUITS               <ul style="list-style-type: none"> <li>• WORKING OF SEMICONDUCTOR DEVICES                   <ul style="list-style-type: none"> <li>• Diodes</li> <li>• Bipolar Junction Transistors</li> <li>• MOSFETS</li> </ul> </li> </ul> </li> <li>❖ Fabrication Process               <ul style="list-style-type: none"> <li>• Oxides, poly silicon and Metal</li> </ul> </li> </ul>	Week 3 Month 1

	<ul style="list-style-type: none"> <li>• Photolithography</li> <li>• Diffusion and Ion implantation</li> <li>• Contacts, Vias</li> <li>• Silicide's, CMP</li> <li>• Self-aligned MOSFET fabrication</li> <li>• N-well and Isolated P-dell (DNW)</li> </ul> <p>❖ CMOS Fabrication process and Introduction to layout</p> <ul style="list-style-type: none"> <li>• CMOS Fabrication Flow</li> <li>• Latch Up</li> <li>• Prevention of latchup</li> <li>• Basic Layout concepts for MOSFETs</li> </ul> <p>❖ CMOS INVERTER</p> <ul style="list-style-type: none"> <li>• Basic circuit and its operation</li> <li>• DC characteristics</li> <li>• Critical voltages in inverter characteristics</li> <li>• Switching characteristics and Power dissipation</li> <li>•</li> </ul>	
	<b>CUSTOM IC LAYOUT</b>	
<b>Module – 4</b> Beginner Custom IC Layouts.	<p>Logic gates and Standard Cells</p> <ul style="list-style-type: none"> <li>• CMOS Logic gates</li> <li>• Driving large loads</li> <li>• Standard cell library</li> <li>• HANDS ON</li> </ul> <p>Standard cell Layout</p> <ul style="list-style-type: none"> <li>• Architecture of standard cell</li> <li>• Abutment and Half design Rule</li> <li>• Standard cell track and its calculation</li> </ul>	Week 4 Month 1
<b>Module 5</b> <b>Project</b>	Project Based on Design and Layout	Week 1,2,3,4 Month 2

**Batch Start:** 1<sup>st</sup> /2<sup>nd</sup> Week of June, 2016.

**Batch Size:** 20 seats.

**Duration:** 1 Month (4 week) Training and 1 Month (4 week) Project.

**Eligibility Criteria:**

1. B.E. or B. Tech from E & C, E & I, E & E, Computer Science/IT.

**Perquisite:-**

1. Knowledge of Advanced and Basic Digital System.

**Required:-**

LAPTOP: – With Minimum Configuration DUAL CORE or i3 or i5 Processor, 2/4 GB DDR3, 500 HDD with window XP or Window 7.

**FEES and Payment Schedule Details:**

**Course Fees: Rs 7500+14.5 % Service Tax.**

**Mode of Payment- Through Cheque or Cash.**

**\*END\***