PINE TRAINING ACADEMY

Course Module

YOUR CAREER, OUR PASSION

6 Month Certified Course In FPGA System Design.

Address

D-557, Govindpuram,
Ghaziabad, U.P., 201013,
India

+91 9999 0 37484

vaibhav.mishra@pinetrainingacademy.com

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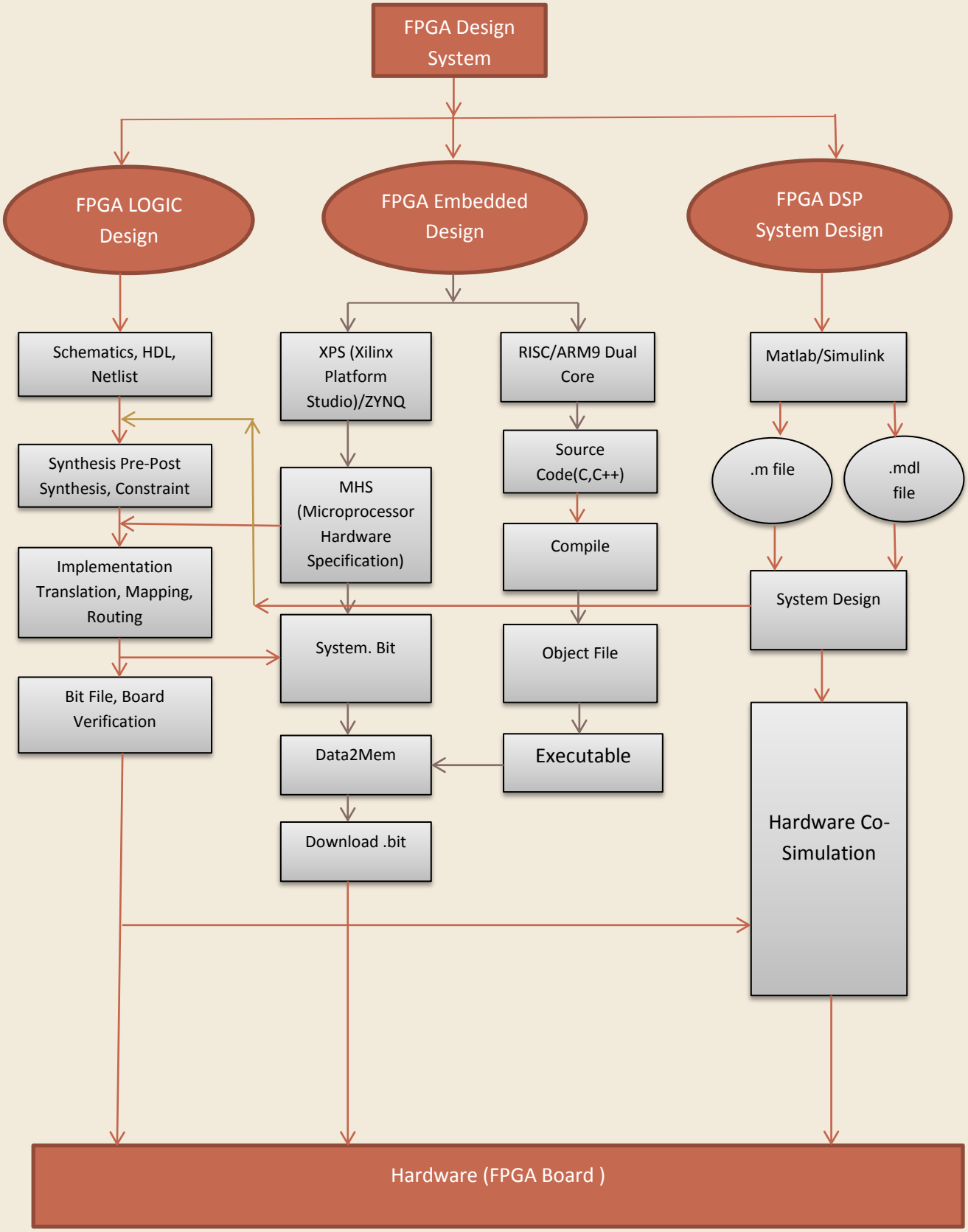
FPGA Design System
FPGA LOGIC Design
FPGA Embedded Design
FPGA DSP System Design
Schematics, HDL, Netlist
Synthesis Pre-Post Synthesis, Constraint
Implementation Translation, Mapping, Routing
Bit File, Board Verification
XPS (Xilinx Platform Studio)/ZYNQ
MHS (Microprocessor Hardware Specification)
System. Bit
Data2Mem
Download .bit
RISC/ARM9 Dual Core
Source Code(C,C++)
Compile
Object File
Executable
Matlab/Simulink
.m file
.mdl file
System Design
Hardware Co-Simulation
Hardware (FPGA Board)

Highlights

- Digital Logic Fundamental.
- Advanced FPGA architecture & Latest Xilinx Tools Flow like PlanAhead Vivado for Logic Design.
- Hardware Programming Language – VHDL.
- Software Programming Language – C and Xilinx Embedded C.
- Introduction of Xilinx Based Semiconductor Application and detail study.
- Introduction to ZYNQ and Xilinx Tools like Vivado System Edition for Embedded Design.
- Advanced Embedded System on ZYNQ.
- Basic of Embedded Linux and Writing Device drivers.
- Development of Embedded Linux System on ZYNQ.
- Development of FPGA based Signal Processing System Design using Xilinx System Generator.
- Development of FPGA based Communication System Design and Image Processing using Xilinx System Generator.
- Industrial Projects.
- Test and Interview Series after completion of every module.
- Visit from Industry.
- Personality Development program and preparation of Interview and Resume.

Main Syllabus

FPGA SYSTEM DESIGN.		
Main Module	**FPGA LOGIC System Design.**	**Duration**

Module -1 Digital System Design.	❖ Digital System Design:-
	• Introduction to Digital System.
	  ○ Number System
	  ○ Digital Logic Levels
	• Digital Logic Circuits.
	  ○ Combinational Logic Circuit.
	  ○ Sequential Logic Circuit.
	• Schematics Entry.
	• FSM.
	• Timing Fundamental.
	• Assignment of Industrial Project.
	• Test and Interview Series.
		2 Week.

Module -2 Introduction of FPGA and Its Resources.	❖ FPGA: - Xilinx Spartan 6/Virtex 6 Basic FPGA Architecture. • CLB. • Routing. • LUT. • Slices. • Wide Multiplexer. • Carry Logic. • Flip Flop and Latches. • CLB Control Signal. • Slices. • I/O Bank Structure. • I/O Versatility. • I/O Electrical. • IOB Element. • IOB Logical Resources. • Global and I/O Clock network (Spartan 6). • Clock buffer and their connection to I/O Resources. • DCM capabilities (Spartan 6). • CMT/PLL (Virtex 6). • Distributes, FIFO and block Memory Resources (Spartan 6/ Virtex 6). • Memory Controller Block (Spartan 6).	1 Week.

	• Configuration. • DSP Slices. • High Speed Transceivers. • PCI Express. • TEMAC • System Monitor. ❖ Exposure of Xilinx Development Board:- • Spartan 6 SP601/SP605 ➢ Interface :- ○ UART. ○ JTAG. ○ FLASH SPI/BPI. ○ DIP Switch. ○ Configuration Mode. ○ LED. ○ LCD. ○ Seven Segment. ○ USB. ○ FMC. ○ Ethernet. ○ PCI. ○ SMA. ○ SFP. • Test and Interview.	
Module – 3 VHDL.	❖ Overview of VHDL. • Introduction. • Code Structure. • Entity. • Architecture. • Predefined Packages. • Port Declaration. • Types of Modelling. • Data Flow Modelling. • Structural Modelling. • Behavioural Modelling. • Mixed Modelling. ❖ Basic Language Construct. • Data Objects. • Data Types. ○ Sub-type. ○ Scalar type. ○ Composite Types. ○ Access Types. ○ Incomplete Type.	3 Week.

- File type.
- Operators.
  - Logical Operators.
  - Relational Operators.
  - Arithmetic Operators.
  - Miscellaneous Operators.

❖ Data Flow Modelling.
- Concurrent Signal Assignment.
- Delta Delay & Multiple drivers.
- Conditional signal assignment: When-else etc.
- Select signal Assignment: with-select.
- Block Statement.
- Concurrent Assertion Statement.

❖ Behavioural Modelling.
- Process Statement.
- Variable & Signal Assignment Statement.
- Wait, If, Case, Null, Loop, Exit & Next Statement.
- Assertion Statement.
- Signal Delays.
  - Inertial Delay.
  - Transport Delay.
- Multiple process & shared variable.

❖ Structural Modelling.
- Component declaration.
- Component Instantiation.
- Resolving Signal Values.

❖ Generic & Configurations.
- Generics.
- Configuration.
- Configuration Specification.
- Configuration Declaration.

❖ Subprograms & Overloading.
- Subprograms.
  - Functions.
  - Procedure.
  - Declarations.
- Subprogram Overloading.
- Operator Overloading.

❖ Package and Libraries.
- Package declaration.
- Package Body.
- Design Libraries.
- Design File.

	• Order of design. ❖ Advanced Features of VHDL. • Entity Statement. • Generate Statement. • Aliases. • Type Conversions. • Guarded Signal. • Attributes. ○ User Defined Attributes. ○ Pre-Defined Attributes. ❖ Aggregate. ❖ Simulation and Test bench. • SDF based simulation. • Writing a Test – bench. ❖ Test and Interview Series.	
Module– 4 FPGA Design Flow – ISE Vivado.	❖ Design technique :- • Simulation. ➢ ISIM. • Synthesis. ➢ Pre- Synthesis Simulation. ➢ Post Synthesis Simulation. ➢ Synthesis Technique. ➢ Analysis of Report. • PlanAhead- ISE. ➢ UCF- I/O Planning. ➢ Timing Constraint. • Implementation. ➢ Translation. ○ Post Translation Simulation. ➢ Mapping. ○ Post Mapping Simulation. ➢ Placement and Routing. ○ Post Placement and Routing Simulation. ➢ Implementation Technique and Analysis of Report at each stage. • Programing. ➢ FPGA Programming. ➢ FLASH Programming. • Project work Continue. • Test and Interview Series.	3 days of Week.

Module-5 Tools Technique ISE/Vivado.	❖ Understanding and Practical Exposure on Tools:- • Coregen/IP catalogue. • Chipscope all type. • PlanAhead. ➢ Area Planning. ➢ Floor Planning. ➢ I/O Planning. • Design Goal and Strategies. • Smart Guide. • Timing Analysis. ➢ SDC Constraint using Vivado. • FPGA Editor. • Power Analyzer. • Smart Xplorer. • iMPACT. • Test and Interview Series.	4 days of Week.
Module-6 FPGA Advanced Technology.	❖ Advanced Study on FPGA Technology. • I/O Technology- MGT/Rocket IO. • Networking-Ethernet. • Interconnect -PCI. • General- FIFO, BRAM. ❖ Schematics Design. • Digital and Analog design concepts. • Schematic symbol creation in Orcad. • Schematic creation and netlisting in Orcad. • Bill of Materials Creation. ❖ Layout Design • Footprint Creation in Allegro. • Placement concepts in board. • Basic routing concepts. • Constraint management. • Gerber Creation.	2 week.

	FPGA Embedded System Design	
Module – 7 FPGA Embedded Architecture.	❖ Embedded System. • Introduction to Embedded System. • Component of Embedded System. • Embedded Processor. ❖ Embedded Support on FPGA • Hard/Soft IPs. • Dedicated hard IPs on FPGA. • BRAM, PCI, Ethernet ❖ ZYNQ Architecture. • Introduction to ZYNQ. • Programmable Logic. • Programmable System. • ARM Cortex A9 architecture. • PS-PL Inter-connection. ❖ Xilinx Tools for Embedded Design. • Embedded Design Flow. • EDK/SDK tool flow. • EDK project creation. • IP Catalogue. • Custom IP integration. ❖ Example/exercise on EDK tools flow on SP605. ❖ Test and Interview Series.	2 week.
Module – 8 Embedded C programing for FPGA.	❖ C programing Steps. • Introduction to cross compilation. • Assembler. • Memory segmentation. • Linkers & executable. ❖ Elements of C programing (review). • Data types. • Function. • Controls. • Loops. • Structure. • File handling. ❖ Xilinx C libraries for FPGA. • Data types. • Function. • Controls • Loops • Structure & file handling. • Test and Interview Series.	3 week.

Module – 9 Embedded System on ZYNQ.	❖ Project Creation in EDK/SDK. ❖ Custom IP and integration lab ❖ Device Drivers. ❖ Example/Exercise on ZYNQ. ❖ Debugging/Profiling of C application	1 week.
Module –10 Embedded Linux on ZYNQ.	❖ Introduction to Embedded Linux. • Embedded Linux system architecture • Linux Kernel Architecture. • Memory Organization. • File system. • Linux Start Sequence. • BSPs. ❖ Embedded Linux Porting Concepts. • Cross-Compilation & GNU cross tool chains. • Porting Road map. • U-boot. • Various format of kernel Image. ❖ Embedded Linux on ZYNQ. • Storage support on ZYNQ. • Booting option for ZYNQ. • Exercise on porting Linux on ZYNQ.	4 week.
	FPGA DSP System Design	
Module –11 Introduction to DSP Tools and Data Types.	• Introduction of Matlab and Simulink. • FPGAs for DSP. • Introduction to System Generator. • Simulink Basics. • Arithmetic Operations. • Fixed Point Format-Signed and Unsigned (with or without binary point). • Gateway In & Out. • Saturation and Wrap in fixed point numbers. • Applications of Round and Truncate in fixed point while arithmetic operations. • Hardware Cost of Saturation, Wrap, Round and Truncation. • Addition, Subtraction, Multiplication, Division, Scaling and Shifting. • Complex arithmetic- Complex multiplication, conjugate etc. • Test and Interview Series.	Weekend 2-DAYS.

Module –12 Block sets Library	• Library Overview • Use of blocks available inside Xilinx Block sets' Library- Basic blocks. • Handshaking blocks- FIFO, BLOCK RAM etc. • Signal Processing Blocks- FFT, FIR etc. • Data storing blocks- ROM. • Black Box- HDL import. • CORDIC • Arithmetic Functions in Circular Co-ordinates. • Implementations. • CORDIC Complier. • Test and Interview Series.	Weekend 2-DAYS.
Module –13 Single Rate & Multi-Rate Filtering	• FIR & IIR Filtering • Sampling, Sub-Sampling, Nyquist-Criterion, Mixing, Quadrature Modulator &I-Q. • Single Rate and Multi-Rate Filters, MAC filters. • Interpolation and Decimation. • Difference between Up sampling, Interpolation, Down sampling and Decimation. • Half- Band Filters and its implementation. • Interpolation FIR filter and its implementation using FDA Tool. • Decimation FIR Filter- with various windowing techniques and its implementation using FDA Tool. • Poly-Phase Filters. • IIR Filter and its implementation using FDA Tool. • Effects of Quantization and importance of ENOB. • LOW PASS CASCADED INTEGRATED COMB (CIC) FILTERS. • Brief Overview of Decimation and Interpolation. • CIC Filters Theory and its Construction. • Interpolation and Decimation with CIC. • CIC Compiler. • Compensation FIR Filter. • Test and Interview Series.	Weekend and weekdays 3-DAYS.

Module -14 Signal Generation within FPGA.	• NUMERICALLY CONTROLLED OSCILLATOR (NCO). • Look Up Table Technique. • DDS Compiler and Phase Truncation techniques. • Sine wave generation using DDS Compiler. • Applications. • Test and Interview Series.	Weekend 2-DAYS.
Module –15 MODEM DESIGN USING DSP.	• INTRODUCTION TO ANALOG AND DIGITAL COMMUNICATION. • Analog modulation schemes. • Analog Transmitter- AM-SSB/AM-DSB/FM. • Analog Receiver- AM-SSB/AM-DSB/FM. • Basic Modulation Schemes like PSK, FSK, QAM, OFDM etc. • PSK based Modulator. • Pulse Shaping and Matched Filtering and its implementation. • PSK based Demodulator. • Communication Link. • Channels and Channel Equalization. • Eb/No Vs BER plots for PSK schemes. • Test and Interview Series.	Weekend and weekdays 3-DAYS.
Module –16 DIGITAL UPCONVERSION & DOWNCONVERSION.	• DUC & DDC DESIGN IN SYSTEM GENERATOR. • Digital Up Convertors and Digital Down Convertors. • Implementation Using either FIR filters or CIC filters, • SNR improvement in DDC. • Test and Interview Series.	Weekend 2-DAYS.
Module –16 HARDWARE CO-SIM.	• HARDWARE CO-SIM & USE OF CHIPSCOPE ANALYZER. • Analyze Design using Timing and Power Report. • Creating HDL. • Creating NGC. • Creating Bit stream. • Analyze Complete Design using CHIPSCOPE ANALYZER. • Hardware Co-Simulations. • Test and Interview Series.	Weekend 2-DAYS.

Batch Start: 28nd July, 2014.

Date of Written Test: 22th July, 2014.

Declaration of Written Test Result: 23rd July 2014.

Date for Interview: 24th, 25th July 2014.

Declaration of Interview result: 26th July 2014.

Date of Registration: 28th July 2014.

Batch Size: 20 seats.

Duration: 6 month, 5 Days in a week, 6-8 hrs. Per day***.

Eligibility Criteria:

1. B.E. or B. Tech /M.Tech with Average 60 % from E & C, E & I, E & E, Computer Science .
2. Written Test and Personal /Technical Interview.

Written test and interview based on both objective and subjective:

1. Basic Analog and Digital Electronics and Engineering Subject.
2. Aptitude Verbal and Non-Verbal.

Perquisite:-

1. Knowledge of Basic Digital System.
2. Knowledge of Basic C, MCU, MPU, Matlab/Simulink and ARM (Optional).

Required:-

LAPTOP: – With Minimum Configuration DUAL CORE or i3 or i5 Processor, 2/4 GB DDR3, 500 HDD with window XP or Window 7.

FEES and Payment Schedule Details:
Course Fees: Rs 60000 +12.36 % Service Tax.
Registration Fees: Rs 5000(At a time of joining, after final selection).
Student can submit fees in two instalment including service tax within one Month.

Mode of Payment- Through Cheque or Cash.

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