PINE TRAINING ACADEMY

Course Module

YOUR CAREER, OUR PASSION

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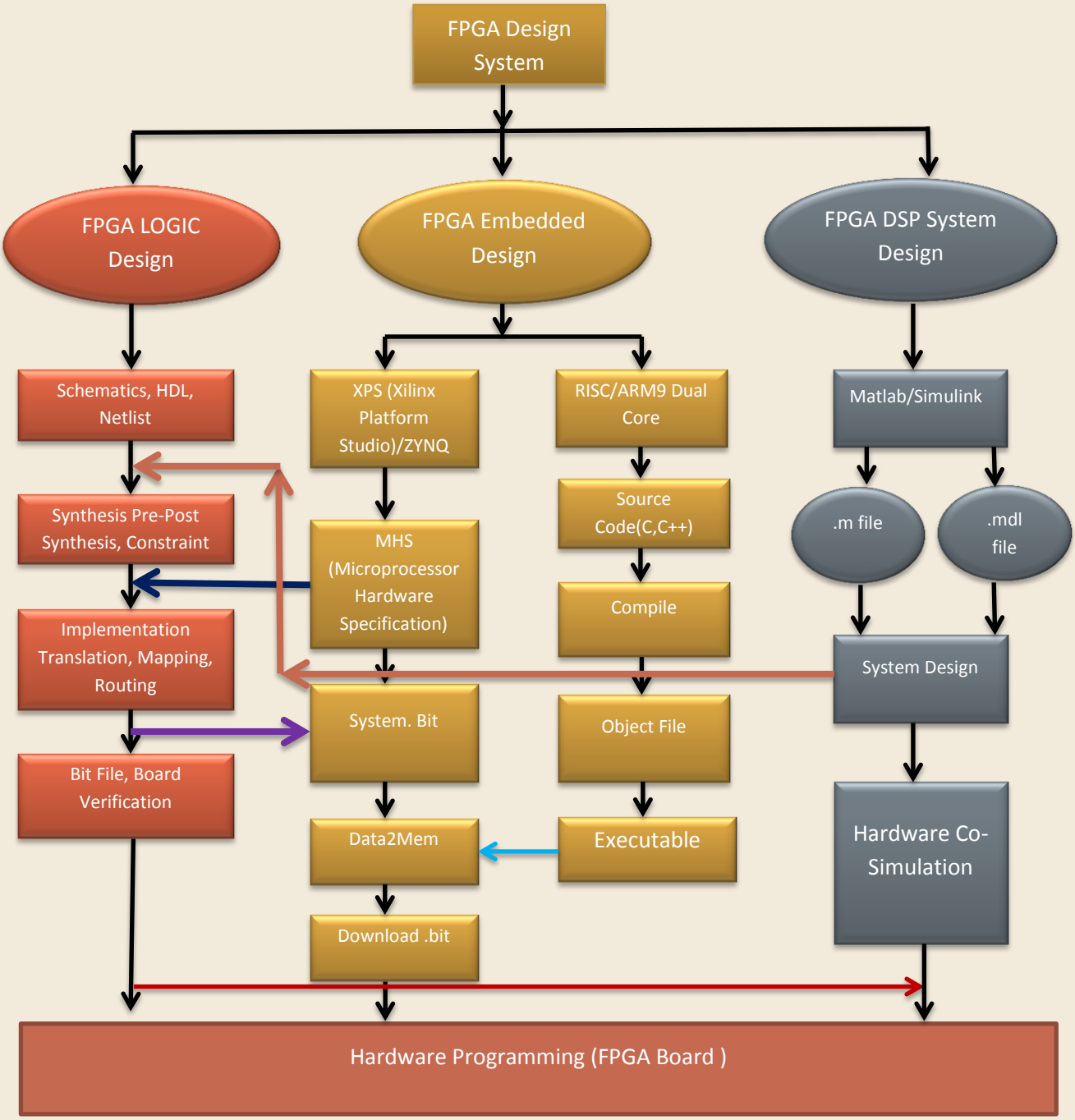
FPGA SYSTEM Design FLOW



Highlights

- Digital Logic Fundamental.
- Advanced FPGA architecture & Latest Xilinx Tools Flow like PlanAhead Vivado for Logic Design.
- Hardware Programming Language – VHDL/Verilog.
- Software Programming Language – Xilinx Embedded C.
- Introduction of Xilinx Based Semiconductor Application and detail study.
- Board and Layout Design – Exposure.
- Exposure on MGT, PCI, Ethernet, FIFO.
- Introduction to ZYNQ and Xilinx Tools like Vivado System Edition for Embedded Design.
- Development of FPGA based Signal Processing System Design using Xilinx System Generator.
- Development of FPGA based Communication System Design using Xilinx System Generator.
- Projects.
- Test and Interview Series after completion of every module.
- Visit from Industry.
- Personality Development program and preparation of Interview and Resume.

Main Syllabus

FPGA SYSTEM DESIGN.		
Main Module	**FPGA LOGIC System Design.**	**Duration**
Module -1 Digital System Design.	❖ Digital System Design:- • Introduction to Digital System. ○ Number System ○ Digital Logic Levels • Digital Logic Circuits. ○ Combinational Logic Circuit. ○ Sequential Logic Circuit. • Schematics Entry. • FSM. • Timing Fundamental. • Test.	
Module – 2 VHDL.	❖ Overview of VHDL. • Introduction. • Code Structure. • Entity. • Architecture. • Predefined Packages. • Port Declaration. • Types of Modelling. • Data Flow Modelling. • Structural Modelling. • Behavioural Modelling. • Mixed Modelling. ❖ Basic Language Construct. • Data Objects. • Data Types. ○ Sub-type. ○ Scalar type. ○ Composite Types. ○ Access Types. ○ Incomplete Type. ○ File type. • Operators. ○ Logical Operators. ○ Relational Operators. ○ Arithmetic Operators. ○ Miscellaneous Operators. ❖ Data Flow Modelling. • Concurrent Signal Assignment.	

	• Delta Delay & Multiple drivers. • Conditional signal assignment: When-else etc. • Select signal Assignment: with-select. • Block Statement. • Concurrent Assertion Statement. ❖ Behavioural Modelling. • Process Statement. • Variable & Signal Assignment Statement. • Wait, If, Case, Null, Loop, Exit & Next Statement. • Assertion Statement. • Signal Delays. ○ Inertial Delay. ○ Transport Delay. • Multiple process & shared variable. ❖ Structural Modelling. • Component declaration. • Component Instantiation. • Resolving Signal Values. ❖ Generic & Configurations. • Generics. • Configuration. • Configuration Specification. • Configuration Declaration. ❖ Subprograms & Overloading. • Subprograms. ○ Functions. ○ Procedure. ○ Declarations. • Subprogram Overloading. • Operator Overloading. ❖ Package and Libraries. • Package declaration. • Package Body. • Design Libraries. • Design File. • Order of design. ❖ Advanced Features of VHDL. • Entity Statement. • Generate Statement. • Aliases. • Type Conversions. • Guarded Signal.	

	• Attributes.
	  ○ User Defined Attributes.
	  ○ Pre-Defined Attributes.
	❖ Aggregate.
	❖ Simulation and Test bench.
	• SDF based simulation.
	• Writing a Test – bench.
	❖ Test and Interview Series.	

Module – 4 Verilog	❖ **Introduction to Verilog course objective.** • Introduction: Reasons for using the Hardware Language. • Hierarchical Design. • Types of Simulators, Compilation, and Synthesis. ❖ **Module** • Structure of Basic Verilog Program. • Defining Module: Port list, Port modes. • Parameters • Instance Types: - Location ❖ **Data Types** • Value Set. • Types of NET. • Strength. • Types of REG: integer, real, time. • Parameters and Parameters Overriding. • Number Representation. ❖ **Data Flow** • Continuous Assignments. • Implicit Continuous Assignment. ❖ **Procedural Blocks** • Always in Synthesis Writing. • Always in Simulation Writing. • Initial: Structure and Example • Intra Assignments. • Language Statements • If else • Case • Loop(while, repeat, forever, for)	

	• Assign deassign • @, #, $ • Lexical Conventions ❖ **Language Operators.** • Concatenation and Replication. • Case Sensitivity. • Identifiers. • Escape Identifiers. • String. • Comments. • Strings. • Comments ❖ **State Machines** • Mealy • Moore. • One Hot ❖ **Gate Level** • Primitives in Verilog • Display Messages • Advanced Writing Simulation • Display Messages • Functions and tasks ❖ Writing a Test – bench. ❖ Test and Interview Series.	
Module -5 Introduction of FPGA and Its Resources.	❖ FPGA: - Xilinx Spartan 6/Virtex 6 Basic FPGA Architecture. • CLB architecture. • LUT architecture. • Slices. • Wide Multiplexer. • I/O Bank Structure. • Clock Managers. • CMT/PLL (Virtex 6). • Block RAM Memories. • External Memory Controller Block (Spartan 6). • Configuration. • DSP Slices. • High Speed Transceivers. • PCI Express. • TEMAC	

	• System Monitor. ❖ Exposure of Xilinx Development Board:- • Spartan 6 SP601/SP605 ➢ Interface :- ○ UART. ○ JTAG. ○ FLASH SPI/BPI. ○ DIP Switch. ○ Configuration Mode. ○ LED. ○ LCD. ○ Seven Segment. ○ USB. ○ FMC. ○ Ethernet. ○ PCI. ○ SMA. ○ SFP. • Test and Interview.	
Module– 6 FPGA Design Flow – ISE Vivado.	❖ Design technique :- • Simulation. ➢ ISIM. • Synthesis. ➢ Pre- Synthesis Simulation. ➢ Post Synthesis Simulation. ➢ Synthesis Technique. ➢ Analysis of Report. • PlanAhead- ISE. ➢ UCF- I/O Planning. ➢ Timing Constraint. • Implementation. ➢ Translation. ○ Post Translation Simulation. ➢ Mapping. ○ Post Mapping Simulation. ➢ Placement and Routing. ○ Post Placement and Routing Simulation. ➢ Implementation Technique and Analysis of Report at each stage. • Programing. ➢ FPGA Programming. ➢ FLASH Programming.	

	• Project work Continue. • Test and Interview Series.	
Module-7 Tools Technique ISE/Vivado.	❖ Understanding and Practical Exposure on Tools:- • Coregen/IP catalogue. • Chipscope all type. • PlanAhead. ➢ Area Planning. ➢ Floor Planning. ➢ I/O Planning. • Design Goal and Strategies. • Smart Guide. • Timing Analysis. ➢ SDC Constraint using Vivado. • Power Analyzer. • Smart Xplorer. • iMPACT. • Test and Interview Series.	
Module-8 FPGA Advanced Technology.	❖ Advanced Study on FPGA Technology. • I/O Technology- MGT/Rocket IO. • Networking-Ethernet. • Interconnect -PCI. • General- FIFO, BRAM. ❖ Schematics Design. • Digital and analog design concepts. • Schematic symbol creation in Orcad. • Schematic creation and netlisting in Orcad. • Bill of Materials Creation. ❖ Layout Design • Footprint Creation in Allegro. • Placement concepts in board. • Basic routing concepts. • Constraint management. • Gerber Creation.	

	FPGA Embedded System Design	
Module – 9 FPGA Embedded Architecture.	❖ Embedded System. • Introduction to Embedded System. • Component of Embedded System. • Embedded Processor. ❖ Embedded Support on FPGA • Hard/Soft IPs. • Dedicated hard IPs on FPGA. • BRAM, PCI, Ethernet ❖ ZYNQ Architecture. • Introduction to ZYNQ. • Programmable Logic. • Programmable System. • ARM Cortex A9 architecture. • PS-PL Inter-connection. ❖ Xilinx Tools for Embedded Design. • Embedded Design Flow. • EDK/SDK tool flow. • EDK project creation. • IP Catalogue. • Custom IP integration. ❖ Xilinx C libraries for FPGA. • Data types. • Function. • Controls • Loops • Structure & file handling. ❖ Example/exercise on EDK tools flow on SP605. ❖ Test and Interview Series.	
Module – 10 Embedded System on ZYNQ.	❖ Project Creation in EDK/SDK. ❖ Custom IP and integration lab ❖ Device Drivers. ❖ Example/Exercise on ZYNQ – ZED Board and AVNET ZYNQ Development board Z7010.	

	FPGA DSP System Design	
Module –11 Introduction to DSP Tools and Data Types.	• Introduction of Matlab and Simulink. • FPGAs for DSP. • Introduction to System Generator. • Simulink Basics. • Arithmetic Operations. • Fixed Point Format-Signed and Unsigned (with or without binary point). • Gateway In & Out. • Saturation and Wrap in fixed point numbers. • Applications of Round and Truncate in fixed point while arithmetic operations. • Hardware Cost of Saturation, Wrap, Round and Truncation. • Addition, Subtraction, Multiplication, Division, Scaling and Shifting. • Complex arithmetic- Complex multiplication, conjugate etc. • Test and Interview Series.	
Module –12 Block sets Library	• Library Overview • Use of blocks available inside Xilinx Block sets' Library- Basic blocks. • Handshaking blocks- FIFO, BLOCK RAM etc. • Signal Processing Blocks- FFT, FIR etc. • Data storing blocks- ROM. • Black Box- HDL import. • CORDIC • Arithmetic Functions in Circular Co-ordinates. • Implementations. • CORDIC Complier. • Test and Interview Series.	
Module –13 Single Rate & Multi-Rate Filtering	• FIR & IIR Filtering • Sampling, Sub-Sampling, Nyquist-Criterion, Mixing, Quadrature Modulator &I-Q. • Single Rate and Multi-Rate Filters, MAC filters. • Interpolation and Decimation.	

	• Difference between Up sampling, Interpolation, Down sampling and Decimation. • Half- Band Filters and its implementation. • Interpolation FIR filter and its implementation using FDA Tool. • Decimation FIR Filter- with various windowing techniques and its implementation using FDA Tool. • Poly-Phase Filters. • IIR Filter and its implementation using FDA Tool. • Effects of Quantization and importance of ENOB. • LOW PASS CASCADED INTEGRATED COMB (CIC) FILTERS. • Brief Overview of Decimation and Interpolation. • CIC Filters Theory and its Construction. • Interpolation and Decimation with CIC. • CIC Compiler. • Compensation FIR Filter. • Test and Interview Series.	
Module -14 Signal Generation within FPGA.	• NUMERICALLY CONTROLLED OSCILLATOR (NCO). • Look Up Table Technique. • DDS Compiler and Phase Truncation techniques. • Sine wave generation using DDS Compiler. • Applications. • Test and Interview Series.	
Module –15 MODEM DESIGN USING DSP.	• INTRODUCTION TO ANALOG AND DIGITAL COMMUNICATION. • Analog modulation schemes. • Analog Transmitter- AM-SSB/AM-DSB/FM. • Analog Receiver- AM-SSB/AM-DSB/FM. • Basic Modulation Schemes like PSK, FSK, QAM, OFDM etc. • PSK based Modulator. • Pulse Shaping and Matched Filtering and its implementation. • PSK based Demodulator.	

	• Communication Link. • Channels and Channel Equalization. • Eb/No Vs BER plots for PSK schemes. • Test and Interview Series.		
Module –16 DIGITAL UPCONVERSION & DOWNCONVERSION.	• DUC & DDC DESIGN IN SYSTEM GENERATOR. • Digital Up Convertors and Digital Down Convertors. • Implementation Using either FIR filters or CIC filters, • SNR improvement in DDC. • Test and Interview Series.		
Module –17 HARDWARE CO-SIM.	• HARDWARE CO-SIM & USE OF CHIPSCOPE ANALYZER. • Analyze Design using Timing and Power Report. • Creating HDL. • Creating NGC. • Creating Bit stream. • Analyze Complete Design using CHIPSCOPE ANALYZER. • Hardware Co-Simulations. • Test and Interview Series.		
Module – 18 Working on Linux or UNIX Enviornment .	❖ UNIX • Basic of UNIX, how different from Windows. • Introduction of SHELL. • File and Directories. • Home Directories Introduction and .cshrc file formation. • Basic Commands-cp,mv,rm,touch,which, mkdir,cat • UNIX sed , cut ,awk,grep (regex),tr commands. • BASH shell scripting, usage of loops, arguments, array.		
Module – 19 TCL	❖ TCL :The command and topics covered in Tcl are • Set • Puts • String cmd & its various options 3.1 compare 3.2 equal 3.3 first 3.4 last		

	3.5 index 3.6 is class 3.7 length 3.8 map 3.9 match 3.10 range 3.11 repeat 3.12 replace 3.13 reverse 3.14 tolower 3.15 toupper 3.16 totitle 3.17 trim 3.18 trimleft 3.19 trimright 3.20 wordstart 3.12 wordend • List and its various options 4.1 lappend 4.2 lindex 4.3 linsert 4.4 llength 4.5 lmap 4.6 lrange 4.7 lrepeat 4.8 lreplace 4.9 lreverse 4.10 lsearch 4.11 lset 4.12 lsort • Concat • Format • Scan • Glob • Global • Incr • Expr • Join • Split • foreach loop • If loop • for loop • switch	

	• while loop • catch • clock • regexp • regsub • Tcl procedures- return,non return, args,optional arguments etc. • file handling:- open & close • file command and its various options • argc,argv,argv0 • arrays • upvar • after • Namespaces • Source • Unset • Exec • Exit • Flush • Time • Break • Continue • Read ❖ Test and Interview.	