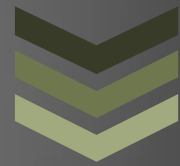


# PINE TRAINING ACADEMY



## Course Module

YOU'RE CAREER, OUR PASSION

Summer Training Program on System  
Verilog

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4/26/2016



Pine Training Academy

## Summer Training Program on Embedded System.

Module	Detailed Syllabus	Duration
<b>Module-1</b> <b>Verilog</b>	<p><b>Lec -1</b></p> <ul style="list-style-type: none"> <li>• Introduction to Verilog and history.</li> <li>• HDL vs. Programming Languages basic differences.</li> <li>• Modeling Styles.</li> <li>• Gate Level Modeling.</li> <li>• Writing a test bench.</li> </ul> <p><b>Hands-on</b></p> <ul style="list-style-type: none"> <li>• Make a half adder using Gate level Modeling.</li> <li>• Verify the validity of the design using Test bench.</li> <li>• Make a full adder using the above half-adder.</li> <li>• Verify the full adder design using Test bench.</li> </ul> <p><b>Lec-2</b></p> <ul style="list-style-type: none"> <li>• Review of last lecture.</li> <li>• Dataflow modelling.</li> <li>• Data Types.</li> <li>• Operators</li> <li>• Delays</li> </ul> <p><b>Hands-on</b></p> <ul style="list-style-type: none"> <li>• Design a full adder using dataflow modelling.</li> <li>• Verify the validity of the design using Test bench.</li> <li>• Design a Mux using dataflow modelling.</li> <li>• Verify the validity of the design using Test bench.</li> </ul> <p><b>Lec-3</b></p> <ul style="list-style-type: none"> <li>• Review of last lecture.</li> <li>• Behavioural modelling.</li> <li>• Blocking and Non-Blocking assignments.</li> <li>• Procedural Statements.</li> <li>• Functions and Tasks.</li> </ul> <p><b>Hands-on</b></p> <ul style="list-style-type: none"> <li>• Design of D-ff using Verilog behavioural modelling.</li> <li>• Verify the validity of D-ff using test bench.</li> <li>• Design of a counter and related concepts.</li> <li>• Verification of counter using test bench.</li> </ul> <p><b>Lec-4</b></p> <ul style="list-style-type: none"> <li>• The advanced concepts of Verilog.</li> <li>• Functions and Tasks.</li> <li>• FSMs and their implementation.</li> </ul> <p><b>Hands-on</b></p> <ul style="list-style-type: none"> <li>• Design of a traffic light controller.</li> <li>• Verification of its functioning using test bench.</li> </ul>	Week 1,2,3,4- Month 1

<b>Module-2</b> <b>System Verilog</b>	<b>Lec-1</b> <ul style="list-style-type: none"> <li>• Introduction to System Verilog and need of Verification.</li> <li>• Data Types in SV.</li> <li>• Fixed Arrays (Packed/Unpacked).</li> <li>• Dynamic Arrays.</li> <li>• Queues.</li> <li>• Associative Arrays.</li> <li>• Methods related to arrays.</li> </ul> <b>Hands-on.</b> <ul style="list-style-type: none"> <li>• Practical evaluation and understanding of features discussed above.</li> <li>• Discussion and doubt session.</li> </ul> <b>Lec-2</b> <ul style="list-style-type: none"> <li>• Operators in System Verilog.</li> <li>• Tasks and Functions in SV.</li> <li>• Interfaces and Clocking Block.</li> <li>• Program Block.</li> </ul> <b>Hands-on</b> <ul style="list-style-type: none"> <li>• Use of interfaces and clocking block.</li> <li>• The understanding of their impact on the verification.</li> </ul> <b>Lec-3</b> <ul style="list-style-type: none"> <li>• The concepts of Oops in SV.</li> <li>• An example of Class.</li> <li>• Overview of the concepts of Inheritance.</li> <li>• Polymorphism.</li> </ul> <b>Hands-on</b> <ul style="list-style-type: none"> <li>• Evaluation of concepts of Oops through examples.</li> <li>• Discussion of usability of these constructs.</li> </ul> <b>Lec-4</b> <ul style="list-style-type: none"> <li>• The interposes communication concepts.</li> <li>• Semaphores.</li> <li>• Mailboxes</li> </ul> <b>Hands-On</b> <ul style="list-style-type: none"> <li>• Basic examples of Semaphores and Mailboxes.</li> </ul> <b>Lec-5</b> <ul style="list-style-type: none"> <li>• The Advanced Concepts of SV.</li> <li>• Assertions and Coverage.</li> <li>• There usage and implications.</li> </ul> <b>Hands-on</b> <ul style="list-style-type: none"> <li>• The understanding of above concepts through examples.</li> </ul>	<b>Week</b> <b>1,2,3,4</b> <b>Month 2</b>
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**Batch Start:** 1<sup>st</sup> /2<sup>nd</sup> Week of June, 2016.

**Batch Size:** 20 seats.

**Duration:** 1 Month (4 week) Training and 1 Month (4 week) Project.

**Eligibility Criteria:**

1. B.E. or B. Tech from E & C, E & I, E & E, Computer Science/IT.

**Perquisite:-**

1. Knowledge of Advanced and Basic Digital System.

**Required:-**

LAPTOP: – With Minimum Configuration DUAL CORE or i3 or i5 Processor, 2/4 GB DDR3, 500 HDD with window XP or Window 7.

**FEES and Payment Schedule Details:**

**Course Fees: Rs 10000+14.5 % Service Tax.**

**Mode of Payment- Through Cheque or Cash.**

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