PINE TRAINING ACADEMY

Course Module

YOU'RE CAREER, OUR PASSION

Summer Training Program on System Verilog

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4/26/2016

Pine Training Academy

Summer Training Program on Embedded System.		
Module	**Detailed Syllabus**	**Duration**
Module–1 **Verilog**	**Lec -1** • Introduction to Verilog and history. • HDL vs. Programming Languages basic differences. • Modeling Styles. • Gate Level Modeling. • Writing a test bench. **Hands-on** • Make a half adder using Gate level Modeling. • Verify the validity of the design using Test bench. • Make a full adder using the above half-adder. • Verify the full adder design using Test bench. **Lec-2** • Review of last lecture. • Dataflow modelling. • Data Types. • Operators • Delays **Hands-on** • Design a full adder using dataflow modelling. • Verify the validity of the design using Test bench. • Design a Mux using dataflow modelling. • Verify the validity of the design using Test bench. **Lec-3** • Review of last lecture. • Behavioural modelling. • Blocking and Non-Blocking assignments. • Procedural Statements. • Functions and Tasks. **Hands-on** • Design of D-ff using Verilog behavioural modelling. • Verify the validity of D-ff using test bench. • Design of a counter and related concepts. • Verification of counter using test bench. **Lec-4** • The advanced concepts of Verilog. • Functions and Tasks. • FSMs and their implementation. **Hands-on** • Design of a traffic light controller. • Verification of its functioning using test bench.	Week 1,2,3,4-Month 1

Module-2 System Verilog	**Lec-1** • Introduction to System Verilog and need of Verification. • Data Types in SV. • Fixed Arrays (Packed/Unpacked). • Dynamic Arrays. • Queues. • Associative Arrays. • Methods related to arrays. **Hands-on.** • Practical evaluation and understanding of features discussed above. • Discussion and doubt session. **Lec-2** • Operators in System Verilog. • Tasks and Functions in SV. • Interfaces and Clocking Block. • Program Block. **Hands-on** • Use of interfaces and clocking block. • The understanding of their impact on the verification. **Lec-3** • The concepts of Oops in SV. • An example of Class. • Overview of the concepts of Inheritance. • Polymorphism. **Hands-on** • Evaluation of concepts of Oops through examples. • Discussion of usability of these constructs. **Lec-4** • The interposes communication concepts. • Semaphores. • Mailboxes **Hands-On** • Basic examples of Semaphores and Mailboxes. **Lec-5** • The Advanced Concepts of SV. • Assertions and Coverage. • There usage and implications. **Hands-on** • The understanding of above concepts through examples.	Week 1,2,3,4 Month 2

Batch Start: 1st /2nd Week of June, 2016.

Batch Size: 20 seats.

Duration: 1 Month (4 week) Training and 1 Month (4 week) Project.

Eligibility Criteria:

1. B.E. or B. Tech from E & C, E & I, E & E, Computer Science/IT.

Perquisite:-

1. Knowledge of Advanced and Basic Digital System.

Required:-

LAPTOP: – With Minimum Configuration DUAL CORE or i3 or i5 Processor, 2/4 GB DDR3, 500 HDD with window XP or Window 7.

FEES and Payment Schedule Details:
Course Fees: Rs 10000+14.5 % Service Tax.

Mode of Payment- Through Cheque or Cash.

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