

Method We follow- How to Get Entry Pass in SEMICODUCTOR Industries for 3rd year engineering

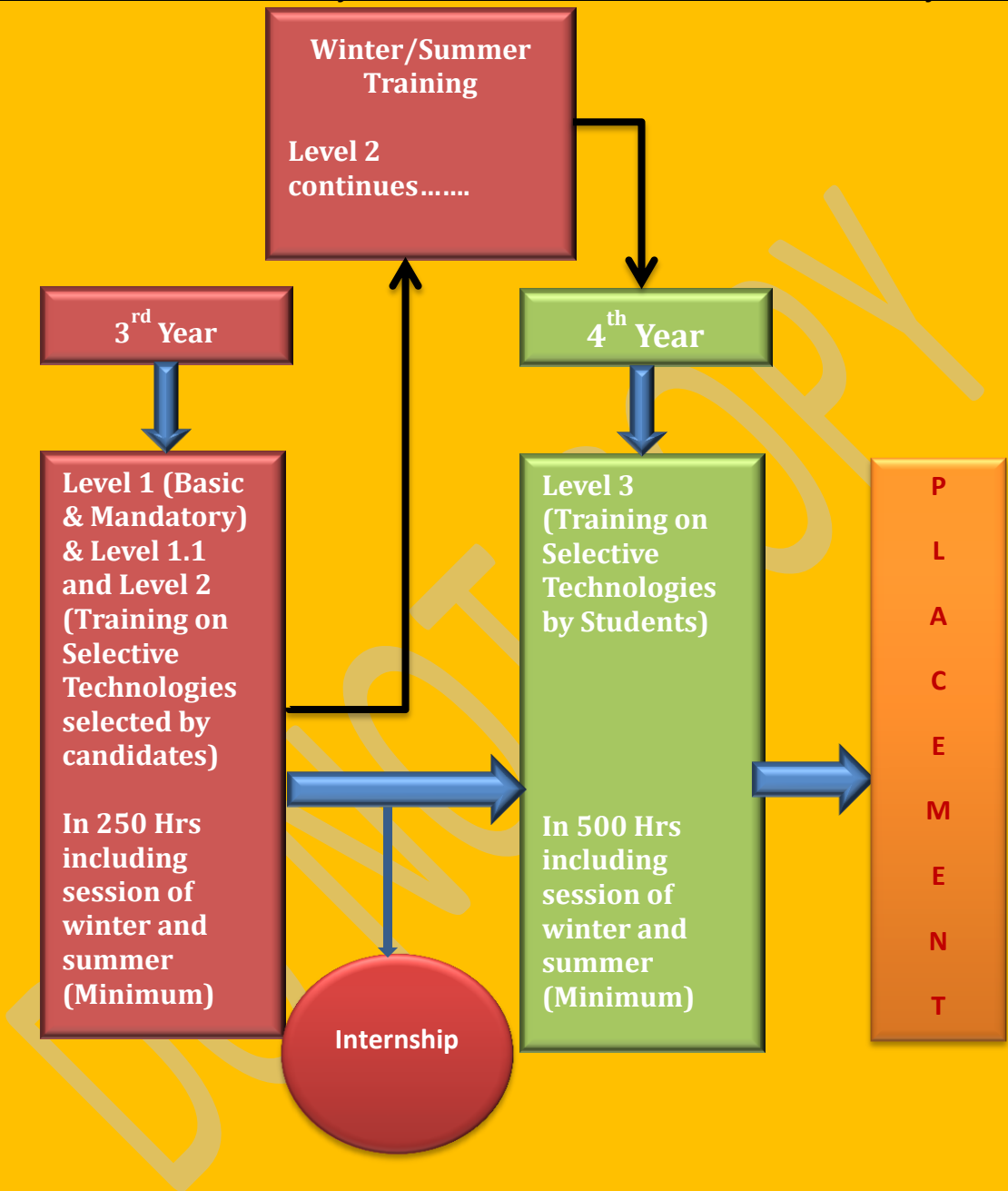


FIG-3

ASIC Schematics Design & Layout

Course Structure for 3rd year only

| Analog (20 Hrs) Module-1 | Digital (20 Hrs) Module -2 | Programming (50 Hrs) Module -3 | FPGA Architecture (20 Hrs) Module -4 |
|---|--|---|--|
| <ul style="list-style-type: none"> • RLC • KCL/KVL • Semiconductor Devices Fundamental • Layout Concept • Electromigration • ESD • Sheet Resistance • Coupling Capacitance fundamental • MOSFET Fundamental • Fabrication Process and Layout Concept. • Analog Fundamental • CMOS Inverter Fundamental • Differential Amplifier • Advanced Digital Topic wrt to written test and Interview. FSM Counter Register FIFO • Timing Fundamental (STA) | <p>Digital Electronics</p> <ul style="list-style-type: none"> • Boolean Algebra • Karnaugh Map • Logic Gates • Numbers system • Combinational Circuits • Sequential Circuits • FSM • Tutorial • HANDS ON (All gates, combinational and sequential circuit's simulation on Xilinx ISE Design and Vivado Design Suite). • Project using Schematics – CRC, Parity Checker, Boot Multiplier, FIFO and Memory etc. | <p>Verilog</p> <ul style="list-style-type: none"> • Introduction Module • Data Types and test Bench • Data Flow and Test Bench. • Gate level and Test Bench. • Procedural Blocks and Test Bench. • Language Operator • Coding Technique. • Synthesis wrt to coding. • Optimization wrt to coding. • Hands on Synthesizable coding technique. • Project – Simulation based project like FIFO etc. and HW based Project like Display and LED control on XILINX Artix 7 board. | <p>Module D-10 Hours- FPGA</p> <ul style="list-style-type: none"> • CLB architecture. • LUT architecture. • Slices. • Wide Multiplexer. • I/O Bank Structure. • Clock Managers. • CMT/PLL (Virtex 6). • Block RAM Memories. • DSP Slices. • Working on FPGA Spartan 6 and Artix 7 Development board with real time project. |

ASIC Schematics Design & Layout

Course Structure for 4th year

| Scripting (60 Hrs) Module -9 | Analog Design (70 Hrs) Module -10 | Layout - (70 Hrs) Module -11 | Project Module -12 |
|--|---|--|---|
| <ul style="list-style-type: none"> • TCL :The command and topics covered in Tcl are • Set • Puts • String cmd & its various options • List and its various options • Tcl procedures- return,non return, args,optional arguments etc. • file handling:- open & close • file command and its various options • | <ul style="list-style-type: none"> • OPAMPS & its Design Concept | <ul style="list-style-type: none"> • Standard Cell Layout • FULL Custom Analog Layout Concept. | <ul style="list-style-type: none"> • Single Stage Differential OPAMPS Design. • Two Stage OPAMPS • Level Shifter |
| <p>UNIX</p> <ul style="list-style-type: none"> • Basic of UNIX, how different from Windows. • Introduction of SHELL. • File and Directories. • Home Directories Introduction and .cshrc file formation. • Basic Commands- cp,mv,rm,touch,which, mkdir,cat • UNIX sed , cut ,awk,grep (regex),tr commands. • BASH shell scripting, usage of loops, arguments, array. | | | |