Method We follow- How to Get Entry Pass in SEMICODUCTOR Industries for 3rd year engineering

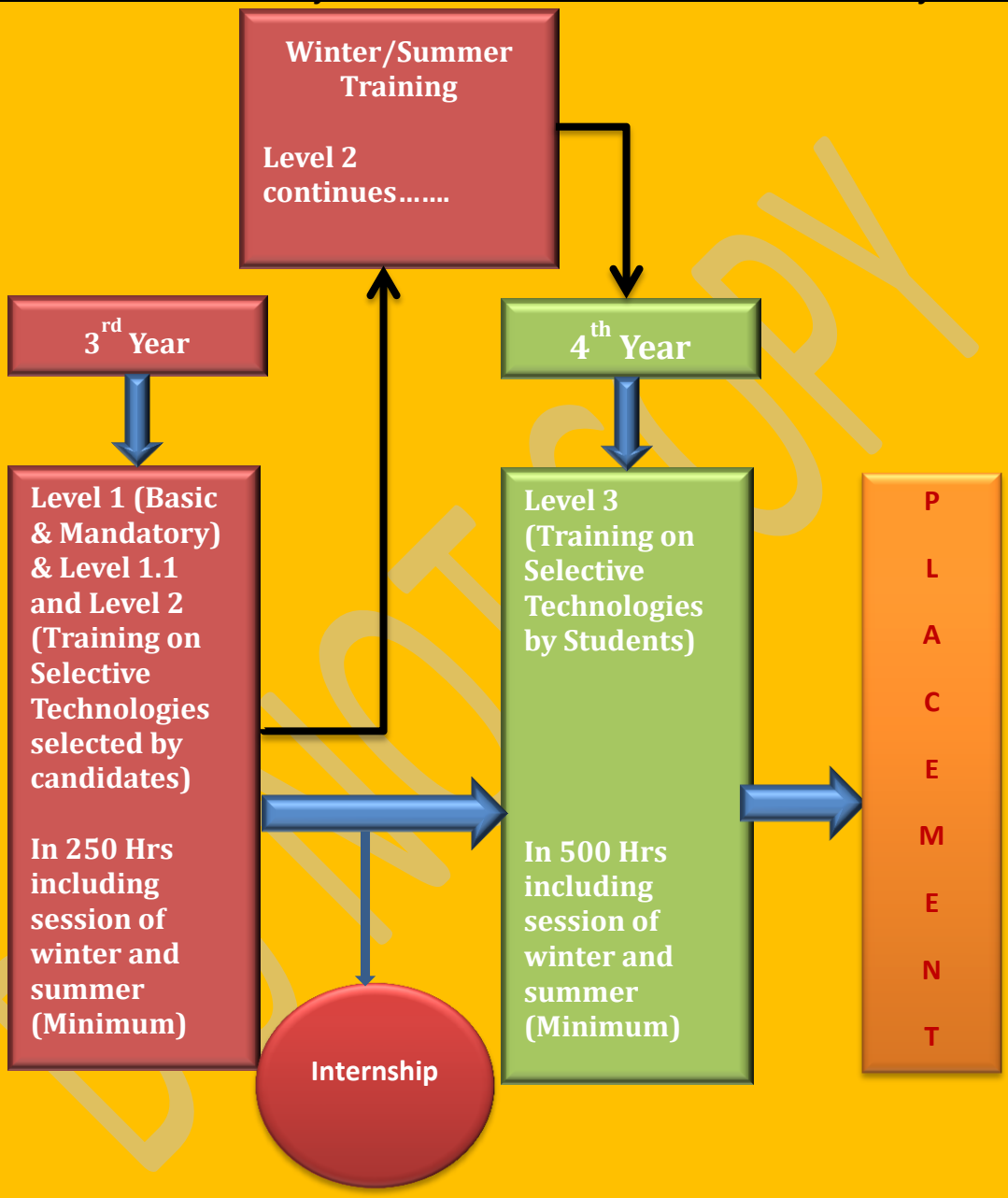

FIG-3

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FPGA System Design

Course Structure for 3rd year

Analog & Digital (20 Hrs)- Module 1	Programing (50 Hrs) Module 2 - RTL	FPGA (10 Hrs) Module -3	FPGA Implementation (20 Hrs) Module -4
Analog Electronics • Diode • BJT • Fabrication Process **Digital Electronics** • Boolean Algebra • Karnaugh Map • Logic Gates • Numbers system • Combinational Circuits • Sequential Circuits • FSM • Tutorial • HANDS ON (All gates, combinational and sequential circuit's simulation on Xilinx ISE Design and Vivado Design Suite). • Project using Schematics – CRC, Parity Checker, Boot Multiplier, FIFO and Memory etc.	**Verilog** • Introduction Module • Data Types and test Bench • Data Flow and Test Bench. • Gate level and Test Bench. • Procedural Blocks and Test Bench. • Language Operator • Coding Technique. • Synthesis wrt to coding. • Optimization wrt to coding. • Hands on Synthesizable coding technique. • Project – Simulation based project like FIFO etc. and HW based Project like Display and LED control on XILINX Artix 7 board.	**Module D-10 Hours-FPGA** • CLB architecture. • LUT architecture. • Slices. • Wide Multiplexer. • I/O Bank Structure. • Clock Managers. • CMT/PLL (Virtex 6). • Block RAM Memories. • DSP Slices. • Working on FPGA Spartan 6 and Artix 7 Development board with real time project.	• Real Time Simulation – Chipscope. • Design using Xilinx Coregen and Vivado IP Integrator. • Timing Analysis using Timing concept on XILINX Tools wrt to timing failure in design. • Working on FPGA Tools feature wrt to Synthesis and Implementation strategies. • FLASH Programing. • Tools Used – XILINX ISE/VIVADO • Modelsim • Altera – Quartus

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Course Structure for 4rd year

Analog/Digital – Advanced (20 Hrs) Module 5	HDL- VHDL – (50 Hrs) Module -6 - RTL	FPGA Embedded Design (75 Hrs) Module-9	DSP FPGA Design (75 Hrs) Module 10
Digital Electronics • Advanced Digital Topic wrt to written test and Interview. FSM Counter Register FIFO • Timing Fundamental (STA) • Working on Linux Environment. • Scripting – TCL **Analog Electronics** • MOSFET Fundamental • Fabrication Process. • Analog Fundamental • CMOS Inverter Fundamental • Differential Amplifier	**VHDL Course Outline** • Entity/Architecture • Logical Operators • Data Types • Concurrent • Sequential Statements • Relational operators • Process, IF THEN WHEN ,CASE, Signals • Describing Clocks • Introducing IEEE 1164 STD_LOGIC • Counter designs • Entity Modes • Making FSM Coding • Enumerated Types • State Machine design Methods • State Machine encoding • Hierarchy • Using PORT MAP to construct design • Package, Function, Configuration. • Using Black Boxes • GERNERICs • Process variables • Process Loops • Generate Statements • Synthesizable coding technique. • The Test Bench • Project both SW and HW implementation on FPGA Boards.	• Introduction to Embedded System. • Introduction to FPGA based Embedded System. • Embedded Support on FPGA. • Processor C for FPGA. • Embedded Processor – RISC 32 Bit. • ZYNQ Architecture. • XILINX Tools for Embedded Design. • Introduction to Embedded Linux. • Embedded Linux Porting Concept. • Embedded Linux on ZYNQ. • Working on FPGA/ZYNQ.	• Introduction of Matlab and Simulink. • FPGAs for DSP. • Introduction to System Generator. • Simulink Basics. • Arithmetic Operations. • Fixed Point Format-Signed and Unsigned (with or without binary point). • Gateway In & Out. • Saturation and Wrap in fixed point numbers. • Applications of Round and Truncate in fixed point while arithmetic operations. • Hardware Cost of Saturation, Wrap, Round and Truncation. • Addition, Subtraction, Multiplication, Division, Scaling and Shifting. • Complex arithmetic- Complex multiplication, conjugate etc. • Library Overview • Use of blocks available inside Xilinx Block sets'

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			Library- Basic blocks. • **Handshaking blocks- FIFO, BLOCK RAM etc.** • **Signal Processing Blocks- FFT, FIR etc.** • **Data storing blocks- ROM.** • **Black Box- HDL import.** • **CORDIC** • **Arithmetic Functions in Circular Co-ordinates.** • **Implementations** • **CORDIC Complier.** • **FIR & IIR Filtering** • **Sampling, Sub-Sampling, NY Quist-Criterion, Mixing, Quadrature Modulator &I-Q.** • **Single Rate and Multi-Rate Filters, MAC filters.** • **Interpolation & Decimation.** • **Difference between Up sampling, Interpolation.** • **Half- Band Filters and its implementation.** • **Interpolation FIR filter and its implementation using FDA Tool.** • **Decimation FIR Filter -with various windowing**

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			techniques and its implementation using FDA Tool. • Poly-Phase Filters. • IIR Filter and its implementation using FDA Tool. • Effects of Quantization and importance of ENOB. • LOW PASS CASCADED INTEGRATED COMB (CIC) FILTERS. • Brief Overview of Decimation and Interpolation. • CIC Filters Theory and its Construction. • Interpolation and Decimation with CIC. • CIC Compiler. • Compensation FIR Filter. • NUMERICALLY CONTROLLED OSCILLATOR (NCO). • Look Up Table Technique. •

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