PINE TRAINING ACADEMY

Course Module

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Certified Online Course in Static Timing Analysis

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For beginner level ***Module Max time 23-25hours***

- What is timing analysis and its importance?
- STA in ASIC design flow and its ROLE
- STA principle and review of libs file
- STA input and output flow diagram
- Different types of timing paths and constraints type
- Overview of different files used for doing STA
    - LIBS
    - SDF
    - SPEF
    - Constraints file
    - Operating conditions (corners and modes information)
- Basic timing constraints information's and development
- Basic concept of setup and Hold
- Delay calculation
    - Timing path delay
    - Interconnect delay model
    - Wire load models
- Equations for calculation of setup and Hold and their Violations with examples
- Understanding of Basic Terminologies related to STA
    - Skew
    - Clock latency and their types
    - Load
    - Delay
- Basic examples to calculate the setup and hold violations

For Medium level ***Module Max time 25hours***

- Brief description of timing libraries and its different types
    - NLDM
    - CCS and CCS noise
- Timing constraints and its development
    - Create clock
    - Generated clock
    - Propagated clocks
    - Input/output delays
    - Clock latency and clock uncertainty
    - Timing exceptions and its precedence (multicycle path, false paths and min/max paths)
    - Clock transition and input transition
    - output load
- Path Delay Calculation
    - Combinational Path Delay
    - Flip-flop to output Path
    - Input to Flip-flop Path
    - Flip-flop to Flip-flop Path
    - Multiple Paths
- Review of timing reports generated by STA tool
- Advance STA concepts with examples
    - All Type of Timing Checks
    - Clock gating
    - Recovery / Removal checks
    - Latches –Time borrowing
- Different methods of timing closure
- Advance examples to solve setup/Hold violations

For Advanced level ***Module Max time 22-25 hours***

- Understanding of Pre layout timing and Post layout timing
- Timing verification
    - Setup timing check with timing reports
        - Flip-flop to Flip-flop Path
        - Input to Flip-flop Path
        - Flip-flop to Output Path
        - Input to Output Path
    - Hold timing check with timing reports
        - Flip-flop to Flip-flop Path
        - Input to Flip-flop Path
        - Flip-flop to Output Path
        - Input to Output Path
- Crosstalk and SI analysis
    - Types of crosstalk
    - Crosstalk delay analysis
    - Timing verification using crosstalk effect
    - Noise avoidance techniques
- PVT conditions and concept of OCV
- CRPR Concepts and its calculation
- Half cycle paths and calculation of Setup/Hold calculation
- Timing across Clock Domains
    - Slow to Fast Clock Domains
    - Fast to Slow Clock Domains
- GBA Vs PBA optimization technique
- Different ways used to fix setup/hold violations in real designs
- Overview of STA by Prime Time (Synopsys) industry standard signoff tool