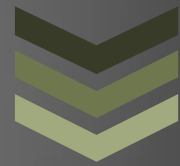


PINE TRAINING ACADEMY



Course Module

YOU'RE CAREER, OUR PASSION

Summer Training Program on System
Verilog

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4/26/2016



Pine Training Academy

Summer Training Program on Embedded System.

Module	Detailed Syllabus	Duration
Module-1 Verilog	<p>Lec -1</p> <ul style="list-style-type: none"> • Introduction to Verilog and history. • HDL vs. Programming Languages basic differences. • Modeling Styles. • Gate Level Modeling. • Writing a test bench. <p>Hands-on</p> <ul style="list-style-type: none"> • Make a half adder using Gate level Modeling. • Verify the validity of the design using Test bench. • Make a full adder using the above half-adder. • Verify the full adder design using Test bench. <p>Lec-2</p> <ul style="list-style-type: none"> • Review of last lecture. • Dataflow modelling. • Data Types. • Operators • Delays <p>Hands-on</p> <ul style="list-style-type: none"> • Design a full adder using dataflow modelling. • Verify the validity of the design using Test bench. • Design a Mux using dataflow modelling. • Verify the validity of the design using Test bench. <p>Lec-3</p> <ul style="list-style-type: none"> • Review of last lecture. • Behavioural modelling. • Blocking and Non-Blocking assignments. • Procedural Statements. • Functions and Tasks. <p>Hands-on</p> <ul style="list-style-type: none"> • Design of D-ff using Verilog behavioural modelling. • Verify the validity of D-ff using test bench. • Design of a counter and related concepts. • Verification of counter using test bench. <p>Lec-4</p> <ul style="list-style-type: none"> • The advanced concepts of Verilog. • Functions and Tasks. • FSMs and their implementation. <p>Hands-on</p> <ul style="list-style-type: none"> • Design of a traffic light controller. • Verification of its functioning using test bench. 	Week 1,2,3,4- Month 1

Module-2 System Verilog	Lec-1 <ul style="list-style-type: none"> • Introduction to System Verilog and need of Verification. • Data Types in SV. • Fixed Arrays (Packed/Unpacked). • Dynamic Arrays. • Queues. • Associative Arrays. • Methods related to arrays. Hands-on. <ul style="list-style-type: none"> • Practical evaluation and understanding of features discussed above. • Discussion and doubt session. Lec-2 <ul style="list-style-type: none"> • Operators in System Verilog. • Tasks and Functions in SV. • Interfaces and Clocking Block. • Program Block. Hands-on <ul style="list-style-type: none"> • Use of interfaces and clocking block. • The understanding of their impact on the verification. Lec-3 <ul style="list-style-type: none"> • The concepts of Oops in SV. • An example of Class. • Overview of the concepts of Inheritance. • Polymorphism. Hands-on <ul style="list-style-type: none"> • Evaluation of concepts of Oops through examples. • Discussion of usability of these constructs. Lec-4 <ul style="list-style-type: none"> • The interposes communication concepts. • Semaphores. • Mailboxes Hands-On <ul style="list-style-type: none"> • Basic examples of Semaphores and Mailboxes. Lec-5 <ul style="list-style-type: none"> • The Advanced Concepts of SV. • Assertions and Coverage. • Their usage and implications. Hands-on <ul style="list-style-type: none"> • The understanding of above concepts through examples. 	Week 1,2,3,4 Month 2
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