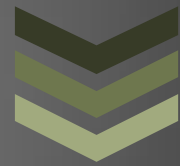


# PINE TRAINING ACADEMY



## Course Module

Digital Logic System Design using  
Gates/Verilog or VHDL and  
Implementation on FPGA.

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Pine Training Academy

## Digital Logic System Design using Gates/Verilog or VHDL and Implementation on FPGA

Module	Detailed Syllabus	Duration
<b>Module– 1</b> Introduction.	<ul style="list-style-type: none"> <li>• Introduction to Pine Training Academy.</li> <li>• Introduction of Semiconductor Industry.</li> <li>• Introduction of VLSI- ASIC &amp; FPGA FLOW.</li> <li>• Study/Revision of Digital System Design.</li> <li>✓ MINIMIZATION OF LOGIC GATES                             <ul style="list-style-type: none"> <li>• BOOLEAN ALGEBRA</li> <li>• K-MAP</li> </ul> </li> <li>✓ LOGIC GATES</li> <li>✓ NAND AND NOR AS A UNIVERSAL GATES</li> <li>✓ COMBINATIONAL CIRCUITS                             <ul style="list-style-type: none"> <li>• HALF ADDER</li> <li>• FULL ADDER</li> <li>• HALF SUBTRACTOR</li> <li>• FULL SUBTRACTOR</li> <li>• SERIAL ADDER</li> <li>• PARALLEL ADDER</li> <li>• LOOK AHEAD CARRY ADDER</li> <li>• MUX, DEMUX</li> <li>• DECODER, ENCODER, PRIORITY ENCODER</li> <li>• COMPARATOR, CODE CONVERTOR</li> </ul> </li> <li>✓ NUMBER SYSTEM</li> <li>✓ SEQUENTIAL CIRCUITS                             <ul style="list-style-type: none"> <li>• FLIP FLOPS</li> <li>• REGISTORS</li> <li>• COUNTERS</li> </ul> </li> <li>✓ MEMORIES</li> <li>✓ INPUT OUTPUT BUFFERS</li> <li>✓ TIMING FUNDAMENTAL</li> <li>✓ CLOCK OSCILLATORS</li> <li>✓ Project: Hardware Design using Digital Components on XILINX ISE Schematics.</li> </ul> <ul style="list-style-type: none"> <li>• Schematics Entry – Practical on ISE.</li> </ul>	Week 1- Month 1

<b>Module – 2</b> <b>FPGA/CPLD:</b> - FPGA Device and FPGA Design Flow.	<ul style="list-style-type: none"> <li>• XILINX FPGA and CPLD Introduction.</li> <li>• Feature.</li> <li>• Architecture.</li> <li>• Packaging.</li> <li>• CLB Overview. <ul style="list-style-type: none"> <li>➤ SLICE</li> <li>➤ LOGIC Cell</li> <li>➤ LUT</li> <li>➤ Carry and Control Logic.</li> </ul> </li> <li>• IOB.</li> <li>• RAM BLOCK.</li> <li>• Multiplier.</li> <li>• Memory.</li> <li>• DCM.</li> <li>• FPGA Nomenclature.</li>   <li>• Written test on Module 2.</li>   <li>• Project Assignment and Project Study: - Industrial Project uses VHDL Implementation on FPGA.</li> </ul>	Week 2 – Month 1
<b>Module – 3</b> <b>HDL- VHDL</b> and Simulation Lab.	<ul style="list-style-type: none"> <li>• Synthesisable VHDL:-XILINX ISE / VIVADO <ul style="list-style-type: none"> <li>➤ Introduction.</li> <li>➤ VHDL Start-up.</li> <li>➤ FPGA Design Flow.</li> <li>➤ Design Entities.</li> <li>➤ Data Types.</li> <li>➤ Combinational Design Method.</li> <li>➤ Sequential Design Method.</li> <li>➤ FSM Synthesis.</li> <li>➤ Memories.</li> <li>➤ Sub-Programs.</li> <li>➤ Parameterised Design.</li> <li>➤ Hierarchical Designs.</li> <li>➤ Test Benches.</li> </ul> </li> <li>• Industrial Project:-Discussion of project start from 1st week and daily 1 hr. discussion on project with student.</li> <li>• Written Test on HDL-VHDL.</li> <li>• Project Work Continue in every week.</li>   <p>Or</p> </ul>	Week 2, 3 and 4 – Month 1

## Synthesisable Verilog

- **Introduction :-**
  - The scope and application of Verilog.
  - Design and tool flow.
  - Types of compilation, Simulation and Synthesis on FPGAs.
- **Module:-**
  - Structure of basic Verilog program.
  - Basic elements of Verilog:-Defining Modules: ports lists, port modes, parameters, Instance type.
- **Language Elements:-**
  - Identifiers, Comments, Compiler Directives.
  - Value Set: integers, real's, strings.
  - Data Type: net, vectored, scalar and registers.
- **Expressions:-**
  - Arithmetic operator.
  - Logical operator.
  - Relational operators.
  - Miscellaneous operators.
- **Modelling:-**
  - Gate Level Modelling.
  - UDP.
  - Data Flow Modelling.
  - Behavioural Modelling:- Procedural Constructs, Timing Controls, Block Statement, Procedural assignment, conditional statement, loop, cases, procedural continuous assignment.
  - Structural Modelling
- **Example Designs:-**
  - Combinational Design.
  - Sequential Design.
- **FSM Synthesis :-**
  - Verilog coding styles for FSMs.
  - State encoding, Unreachable states and input hazards.
- **Memories:-**
  - Array types.
  - Modelling memories.

	<ul style="list-style-type: none"> <li>➤ Implementing ROMs &amp; RAMs.</li> <li>● <b>Advanced Verilog:-</b> <ul style="list-style-type: none"> <li>➤ System Task.</li> <li>➤ Function.</li> <li>➤ Test benches.</li> <li>➤ verification</li> </ul> </li> <li>● Industrial Project:-Discussion of project start from 1st week and daily 1 hr. discussion on project with student.</li> <li>● Written Test on HDL-VHDL.</li> </ul> <p>Project Work (Continue in every week).</p>	
<p><b>Module– 4</b> FPGA Design Flow and Study of FPGA Development board.</p>	<ul style="list-style-type: none"> <li>● Synthesis. <ul style="list-style-type: none"> <li>➤ Pre- Synthesis Simulation.</li> <li>➤ Post Synthesis Simulation.</li> <li>➤ Synthesis Technique.</li> <li>➤ Analysis of Report.</li> </ul> </li> <li>● PlanAhead- ISE. <ul style="list-style-type: none"> <li>➤ UCF.</li> </ul> </li> <li>● Implementation. <ul style="list-style-type: none"> <li>➤ Translation. <ul style="list-style-type: none"> <li>○ Post Translation Simulation.</li> </ul> </li> <li>➤ Mapping. <ul style="list-style-type: none"> <li>○ Post Mapping Simulation.</li> </ul> </li> <li>➤ Placement and Routing. <ul style="list-style-type: none"> <li>○ Post Placement and Routing Simulation.</li> </ul> </li> <li>➤ Implementation Technique and Analysis of Report at each stage.</li> </ul> </li> <li>● Programing. <ul style="list-style-type: none"> <li>➤ FPGA Programming.</li> <li>➤ FLASH Programming.</li> </ul> </li> <li>● Project work Continue.</li> <li>● Written test on Module 4.</li> </ul>	<p>Week 2 Month 1</p>
<p><b>Module – 5.</b> Development Board- Xilinx.</p>	<ul style="list-style-type: none"> <li>● Study of Xilinx Spartan 6 SP605 /SP601 Development Board. <ul style="list-style-type: none"> <li>➤ Study of Interface. <ul style="list-style-type: none"> <li>○ LED.</li> <li>○ Switch.</li> <li>○ Button.</li> <li>○ DIP.</li> <li>○ FLASH.</li> <li>○ UART.</li> </ul> </li> </ul> </li> <li>● Completion of Project, Viva and Hanover of Certificate.</li> </ul>	<p>Week 1,2,3,4- Month 2 – Project based Internship</p>