PINE TRAINING ACADEMY

Course Module

YOUR CAREER, OUR PASSION

10 Month Certified Course in ASIC Design (Analog LAYOUT).

Address

D-557, Govindpuram, Ghaziabad, U.P., 201013, India

+91 9999 0 37484

vaibhava.mishra@pinetrainingacademy.com

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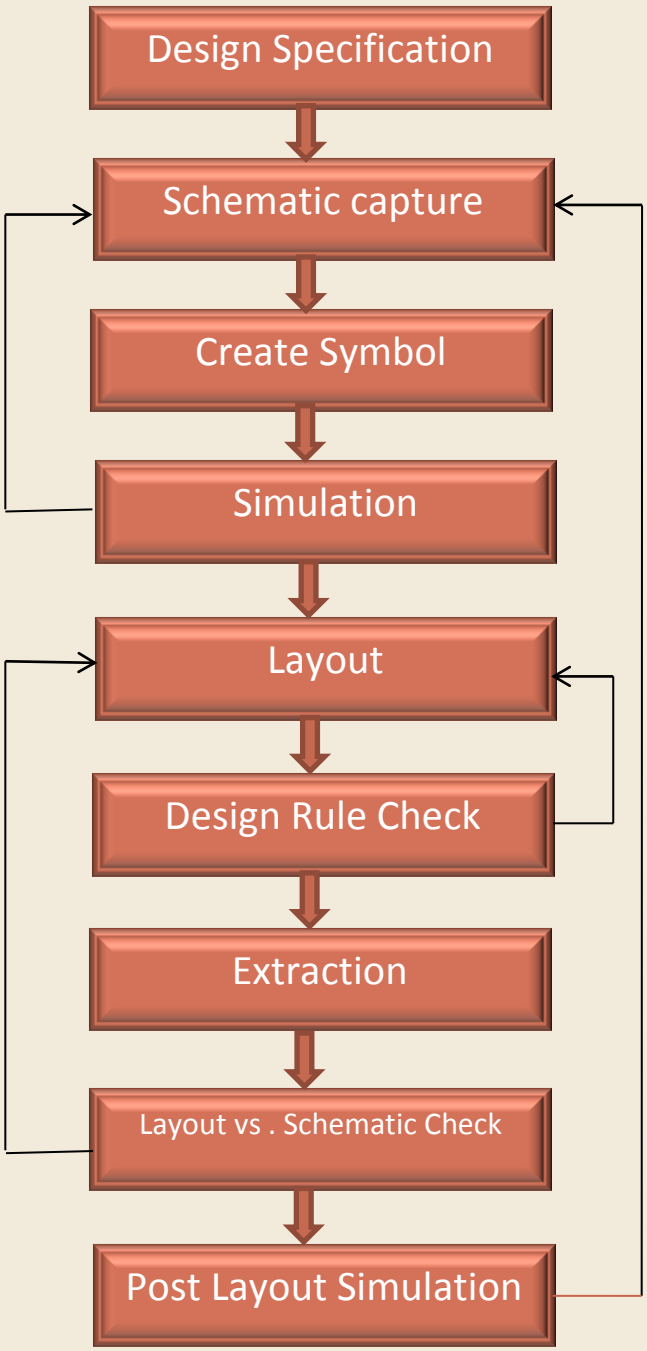
Pine Training Academy

CUSTOM IC FLOW



Highlights

- Digital Logic Fundamental like Basic and Advanced Digital.
- Brief study of FSM and TIMING.
- Basic FPGA Architecture.
- Xilinx Tools Flow like PlanAhead Vivado for Logic Design.
- Hardware Programming Language –Verilog.
- Basic Knowledge of Synthesis, Implementation and Optimization.
- Working knowledge of UNIX Shell and TCL Scripting Language.
- Study of two stage OPAMP.
- Introduction of custom IC layout.
- Fundamental of CMOS Theory, IC Layout , standard cell , Analog
- Introduction to standard cell layout like inverter gate and universal layout.
- Working knowledge of verification like DRC, LVS.
- Industrial Projects.
- Test and Interview Series after completion of every module.
- Visit from Industry.
- Personality Development program and preparation of Interview and Resume.

	ASIC Design (Analog LAYOUT)		
Main Module	**FPGA LOGIC System Design using Verilog**		**Duration**

Module -1 Digital System Design.	❖ Digital System Design:-
	• Introduction to Digital System.
	  ○ Number System
	  ○ Digital Logic Levels
	• Digital Logic Circuits.
	  ○ Combinational Logic Circuit.
	  ○ Sequential Logic Circuit.
	• Schematics Entry.
	• FSM.
	• Timing Fundamental.
	• Assignment of Industrial Project.
	• Test and Interview Series.		

Module – 2 UNIX	❖ UNIX • Basic of UNIX, how different from Windows. • Introduction of SHELL. • File and Directories. • Home Directories Introduction and .cshrc file formation. • Basic Commands-cp,mv,rm,touch,which, mkdir,cat • UNIX sed , cut ,awk,grep (regex),tr commands. • BASH shell scripting, usage of loops, arguments, array.		
Module – 3 TCL	❖ TCL :The command and topics covered in Tcl are • Set • Puts • String cmd & its various options 3.1 compare 3.2 equal 3.3 first 3.4 last 3.5 index 3.6 is class 3.7 length 3.8 map 3.9 match 3.10 range 3.11 repeat 3.12 replace		

	3.13 reverse 3.14 tolower 3.15 toupper 3.16 totitle 3.17 trim 3.18 trimleft 3.19 trimright 3.20 wordstart 3.12 wordend • List and its various options 4.1 lappend 4.2 lindex 4.3 linsert 4.4 llength 4.5 lmap 4.6 lrange 4.7 lrepeat 4.8 lreplace 4.9 lreverse 4.10 lsearch 4.11 lset 4.12 lsort • Concat • Format • Scan • Glob • Global • Incr • Expr • Join • Split • foreach loop • If loop • for loop • switch • while loop • catch • clock • regexp • regsub • Tcl procedures- return,non return, args,optional		

	arguments etc. • file handling:- open & close • file command and its various options • argc,argv,argv0 • arrays • upvar • after • Namespaces • Source • Unset • Exec • Exit • Flush • Time • Break • Continue • Read ❖ Test and Interview.		
Module -4 Introduction of FPGA and Its Resources.	❖ FPGA: - Xilinx Spartan 6/Virtex 6 Basic FPGA Architecture and detail discussion of Components and implementation on project.		
Module – 5 Verilog	❖ **Introduction to Verilog course objective.** • Introduction: Reasons for using the Hardware Language. • Hierarchical Design. • Types of Simulators, Compilation, and Synthesis. ❖ **Module** • Structure of Basic Verilog Program. • Defining Module: Port list, Port modes. • Parameters • Instance Types: - Location ❖ **Data Types** • Value Set. • Types of NET. • Strength.		

- Types of REG: integer, real, time.
- Parameters and Parameters Overriding.
- Number Representation.

❖ **Data Flow**
- Continuous Assignments.
- Implicit Continuous Assignment.

❖ **Procedural Blocks**
- Always in Synthesis Writing.
- Always in Simulation Writing.
- Initial: Structure and Example
- Intra Assignments.
- Language Statements
- If else
- Case
- Loop(while, repeat, forever, for)
- Assign de-assign
- @, #, $
- Lexical Conventions

❖ **Language Operators.**
- Concatenation and Replication.
- Case Sensitivity.
- Identifiers.
- Escape Identifiers.
- String.
- Comments.
- Strings.
- Comments

❖ **State Machines**
- Mealy
- Moore.
- One Hot

❖ **Gate Level**
- Primitives in Verilog
- Display Messages
- Advanced Writing Simulation
- Display Messages

	• Functions and tasks ❖ Writing a Test – bench. ❖ Test and Interview Series.		
Module– 6 FPGA Design Flow	❖ Design technique :- • Simulation. ➢ ISIM. • Synthesis. ➢ Pre- Synthesis Simulation. ➢ Post Synthesis Simulation. ➢ Synthesis Technique. ➢ Analysis of Report.		
Module -7 Schematic Design	1. Basic concepts 1.1 Introduction to R, C, L circuits 1.2 current and voltage sources 1.3 introductions to simulation environment and various types of analysis. 2. 2. Introduction to MOSFET device physics 2.1 MOSFET operation 2.2 input and output characteristics 2.3 regions of operation - linear, saturation, sub threshold region 2.4 MOSFET small signal model 3. 3 Single stage amplifiers 3.1 common source, 3.2 common gate, 3.3 source follower 3.4 source degeneration 4. Operational amplifiers 4.1 Basic current mirror		

	4.2 cascode current mirror 4.3 Single stage differential amplifier 4.4 Two stage op amp 4.5 Frequency response 4.6 Compensation techniques Extra useful topics 1. Simplified CMOS inverter characteristics 2. Flip flop setup/hold explanation 3. Different types of Devices available in silicon technologies		
	CUSTOM IC LAYOUT		
Module – 8 Beginner Custom IC Layouts.	❖ Introduction of R, L, C, Diode, bipolar, MOS. ❖ Basic CMOS theory (layout of p/n mos). ❖ Basic IC Fabrication steps. ❖ Basic concept of Standard cell/ Analog/IO layout. ❖ Brief introduction of Full chip Layout Blocks eg. I/O, memory etc. ❖ Layout of max possible components used in IC Design eg R, C, Diode, CMOS etc. ❖ Test and Interview.		
Module – 9 Intermediate Custom IC LAYOUT	❖ Standard cell layout concept and industry level discussion on it • Grid/Track Calculation • Half Design Rule • Tap or Tapeless Architecture and sharing concept • Inverter and universal gates layout (Standard cell layout) ❖ Test and Interview.		
Module – 10 EXPERT-Custom IC Layout	❖ Analog layout concept and industry level discussion on various topics related to analog layout • Inverter and universal gates layout (analog layout) • Folding, fingering • Latch Up • Electro Migration • Matching (Current Mirror and Diff Amp layout) • Antenna • Static/Active Shielding		

	• IR drop • Double Patterning (LELE, LFLE, SADP) • Via Redundancy • Density and Tiling • Isolated Pwell (DNW) • Physical Verification eg. DRC/LVS/DFM etc. • DRM • ERC and Soft Check ❖ Test and Interview.		