PINE TRAINING ACADEMY

Course Module

YOUR CAREER, OUR PASSION

10 Month Certified Course in ASIC Verification.

Address

D-557, Govindpuram, Ghaziabad, U.P., 201013, India

+91 9999 0 37484

vaibhava.mishra@pinetrainingacademy.com

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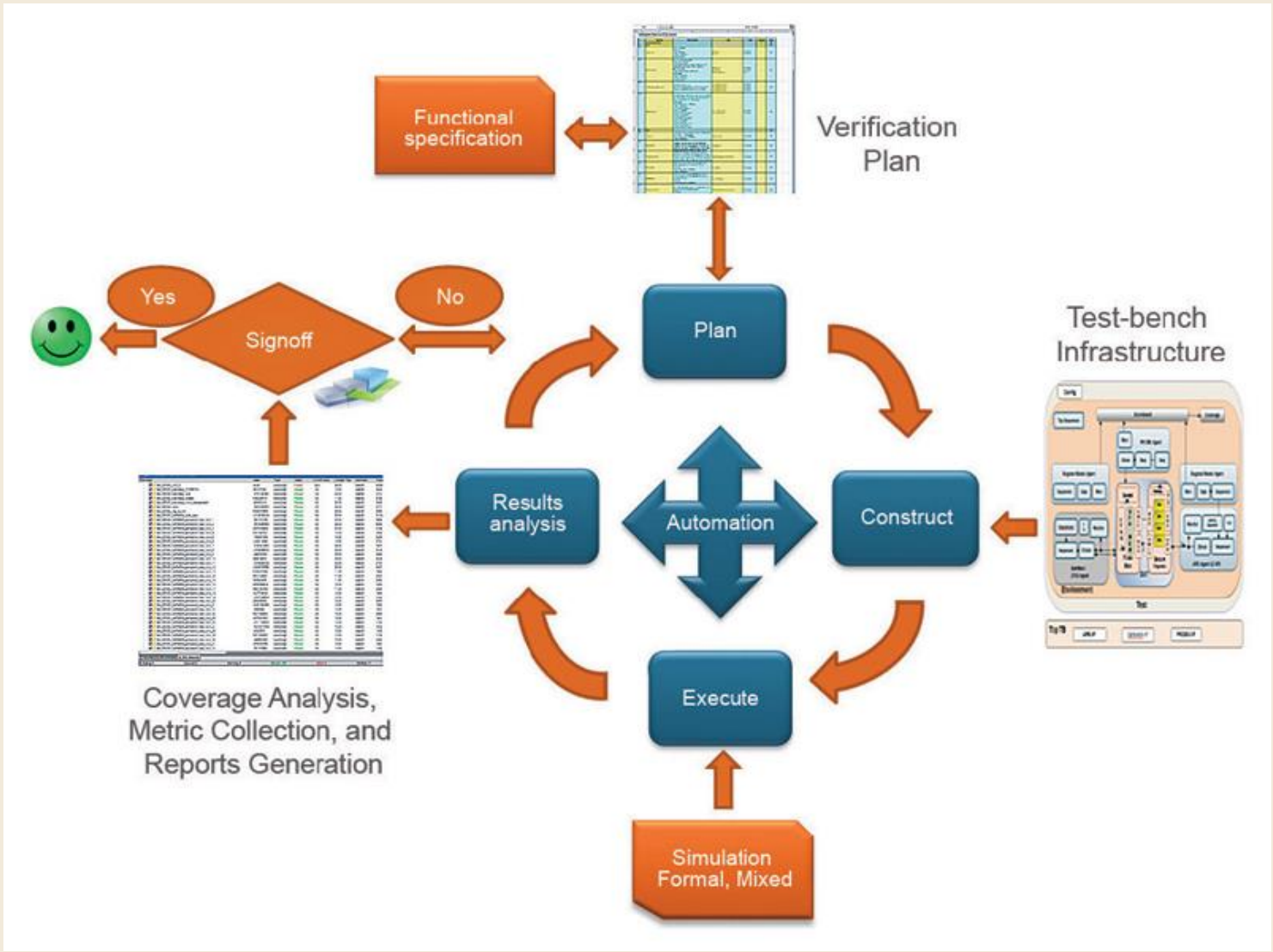
Verification Flow in Design Signoff



Highlights

- Understanding of Black box verification and White box verification
- Understanding of different verification (IP Verification, SoC Verification, Subsystem Verification, Verification IP Design)
- Digital Logic Fundamental like Basic and Advanced Digital.
- Brief Study of C and Object Oriented programming.
- Basic knowledge of Linux and Scripting.
- Hardware Design Language (Verilog).
- Hardware Verification Language (System Verilog)
- Verification Methodology (UVM)
- Brief study of AMBA Bus (APB,AHB,AXI).
- Industrial Project.
- Test and Interview Series after completion of every module.
- Visit from Industry.
- Personality Development program and preparation of Interview and Resume.

	ASIC Verification		
Main Module	**Digital System Design**		

Module -1 Digital System Design.	❖ Digital System Design:-
	• Introduction to Digital System.
	  ○ Number System
	  ○ Digital Logic Levels
	• Digital Logic Circuits.
	  ○ Combinational Logic Circuit.
	  ○ Sequential Logic Circuit.
	• Schematics Entry.
	• FSM.
	• Timing Fundamental.
	• Assignment of Industrial Project.
	• Test and Interview Series.		

Module – 2 UNIX	❖ UNIX • Basic of UNIX, how different from Windows. • Introduction of SHELL. • File and Directories. • Home Directories Introduction and .cshrc file formation. • Basic Commands-cp,mv,rm,touch,which, mkdir,cat • UNIX sed , cut ,awk,grep (regex),tr commands. • BASH shell scripting, usage of loops, arguments, array.		
Module – 3 C, OOP concept	❖ C & Object Oriented Programming • C and Verification • Why C is useful in Verification • Complete C programming language brief • Object oriented programming and Verification • Brief of Object Oriented Programming		
Module -4 HDL(Hardware Design Language)	❖ Hardware Design Language (Verilog). • Need of Verilog • Abstraction Level • Concurrency • Digital Circuit design with Verilog • Need of Verification of HDL design • 4 State & 2 State logic • Top Down & Bottom up design Methodology • Verilog HDL Design Flow		

	• Verilog Syntax and Symantics • Gate level Modelling • Data Flow Modelling • Behavioural Level Modelling • Blocking & Non-blocking assignment • Test & Interview questions		
Module – 5 System Verilog(HVL)	❖ **Introduction to System Verilog course objective.** • Introduction: Reasons for using the Hardware Verification Language. • Benefits of System Verilog in Verification. • System Verilog Data types • Procedural Statements and Routines • Interface & Virtual Interface • Constraint Randomization & Need of Randomization • Threads & Interprocess Communication • Coverage Metric(Code coverage, Functional Coverage) • Callbacks • Cross coverage ❖ Writing a Test – bench. ❖ Test and Interview Series.		
Module– 6 UVM Methodology	❖ Universal Verification Methodology(UVM) • UVM Testbench • UVM Phases • UVM Top-down & Bottom-up approach • UVM Reporting • UVM Transaction • UVM Configuration • UVM Factory • UVM Sequence (also UVM Virtual sequence) • UVM Components(Monitor, Agent, Environment , Sequencer, Driver) • UVM Transaction level Methodology • UVM Callbacks		

Module -7 **AMBA Bus**	❖ Advance Microcontroller Bus Architecture ❖ APB ❖ AHB ❖ AXI ❖ Why AMBA is so important for Verification? ❖ One Project of Verification IP development for any AMBA bus.		5 Week