PINE TRAINING ACADEMY

Course Module

Digital Logic System Design using Gates/Verilog or VHDL and Implementation on FPGA.

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Digital Logic System Design using Gates/Verilog or VHDL and Implementation on FPGA		
Module	**Detailed Syllabus**	**Duration**

Module– 1 Introduction.	• Introduction to Pine Training Academy.
	• Introduction of Semiconductor Industry.
	• Introduction of VLSI- ASIC & FPGA FLOW.
	• Study/Revision of Digital System Design.
	✓ MINIMIZATION OF LOGIC GATES
	  • BOOLEAN ALGEBRA
	  • K-MAP
	✓ LOGIC GATES
	✓ NAND AND NOR AS A UNIVERSAL GATES
	✓ COMBINATIONAL CIRCUITS
	  • HALF ADDER
	  • FULL ADDER
	  • HALF SUBRACTOR
	  • FULL SUBTRACTOR
	  • SERIAL ADDER
	  • PARALLEL ADDER
	  • LOOK AHEAD CARRY ADDER
	  • MUX, DEMUX
	  • DECODER, ENCODER, PRIORITY ENCODER
	  • COMPARATOR, CODE CONVERTOR
	✓ NUMBER SYSTEM
	✓ SEQUENTIAL CIRCUITS
	  • FLIP FLOPS
	  • REGISTORS
	  • COUNTERS
	✓ MEMORIES
	✓ INPUT OUTPUT BUFFERS
	✓ TIMING FUNDAMENTAL
	✓ CLOCK OSCILLATORS
	✓ Project: Hardware Design using Digital Components on XILINX ISE Schematics.
	
	• Schematics Entry – Practical on ISE.
		Week 1-Month 1

Module – 2 FPGA/CPLD:- FPGA Device and FPGA Design Flow.	• XILINX FPGA and CPLD Introduction.
	• Feature.
	• Architecture.
	• Packaging.
	• CLB Overview.
	  ➢ SLICE
	  ➢ LOGIC Cell
	  ➢ LUT
	  ➢ Carry and Control Logic.
	• IOB.
	• RAM BLOCK.
	• Multiplier.
	• Memory.
	• DCM.
	• FPGA Nomenclature.
	
	• Written test on Module 2.
	
	• Project Assignment and Project Study: - Industrial Project uses VHDL Implementation on FPGA.
		Week 2 – Month 1

Module – 3 HDL- VHDL and Simulation Lab.	• Synthesisable VHDL:-XILINX ISE / VIVADO
	  ➢ Introduction.
	  ➢ VHDL Start-up.
	  ➢ FPGA Design Flow.
	  ➢ Design Entities.
	  ➢ Data Types.
	  ➢ Combinational Design Method.
	  ➢ Sequential Design Method.
	  ➢ FSM Synthesis.
	  ➢ Memories.
	  ➢ Sub-Programs.
	  ➢ Parameterised Design.
	  ➢ Hierarchical Designs.
	  ➢ Test Benches.
	• Industrial Project:-Discussion of project start from 1st week and daily 1 hr. discussion on project with student.
	• Written Test on HDL-VHDL.
	• Project Work Continue in every week.
	
	Or
		Week 2, 3 and 4 – Month 1

Synthesisable Verilog

- **Introduction :-**
  - The scope and application of Verilog.
  - Design and tool flow.
  - Types of compilation, Simulation and Synthesis on FPGAs.
- **Module:-**
  - Structure of basic Verilog program.
  - Basic elements of Verilog:-Defining Modules: ports lists, port modes, parameters, Instance type.
- **Language Elements:-**
  - Identifiers, Comments, Compiler Directives.
  - Value Set: integers, real's, strings.
  - Data Type: net, vectored, scalar and registers.
- **Expressions:-**
  - Arithmetic operator.
  - Logical operator.
  - Relational operators.
  - Miscellaneous operators.
- **Modelling:-**
  - Gate Level Modelling.
  - UDP.
  - Data Flow Modelling.
  - Behavioural Modelling:- Procedural Constructs, Timing Controls, Block Statement, Procedural assignment, conditional statement, loop, cases, procedural continuous assignment.
  - Structural Modelling
- **Example Designs:-**
  - Combinational Design.
  - Sequential Design.
- **FSM Synthesis :-**
  - Verilog coding styles for FSMs.
  - State encoding, Unreachable states and input hazards.
- **Memories:-**
  - Array types.

	➢ Modelling memories. ➢ Implementing ROMs & RAMs. • **Advanced Verilog:-** ➢ System Task. ➢ Function. ➢ Test benches. ➢ verification • Industrial Project:-Discussion of project start from 1st week and daily 1 hr. discussion on project with student. • Written Test on HDL-VHDL. Project Work (Continue in every week).	
Module– 4 FPGA Design Flow and Study of FPGA Development board.	• Synthesis. ➢ Pre- Synthesis Simulation. ➢ Post Synthesis Simulation. ➢ Synthesis Technique. ➢ Analysis of Report. • PlanAhead- ISE. ➢ UCF. • Implementation. ➢ Translation. o Post Translation Simulation. ➢ Mapping. o Post Mapping Simulation. ➢ Placement and Routing. o Post Placement and Routing Simulation. ➢ Implementation Technique and Analysis of Report at each stage. • Programing. ➢ FPGA Programming. ➢ FLASH Programming. • Project work Continue. • Written test on Module 4.	Week 2 Month 1
Module – 5. Development Board- Xilinx.	• Study of Xilinx Spartan 6 SP605 /SP601 Development Board. ➢ Study of Interface. o LED. o Switch. o Button. o DIP. o FLASH. o UART. • Completion of Project, Viva and Hanover of Certificate.	Week 1,2,3,4- Month 2 – Project based Internship

Batch Start: 1st /2nd Week of June, 2016.

Batch Size: 20 seats.

Duration: 1 Month (4 week) Training and 1 Month (4 week) Project.

Eligibility Criteria:

1. B.E. or B. Tech from E & C, E & I, E & E, Computer Science/IT.

Perquisite:-

1. Knowledge of Advanced and Basic Digital System.

Required:-

LAPTOP: – With Minimum Configuration DUAL CORE or i3 or i5 Processor, 2/4 GB DDR3, 500 HDD with window XP or Window 7.

FEES and Payment Schedule Details:
Course Fees: Rs 7500+14.5 % Service Tax.

Mode of Payment- Through Cheque or Cash.

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