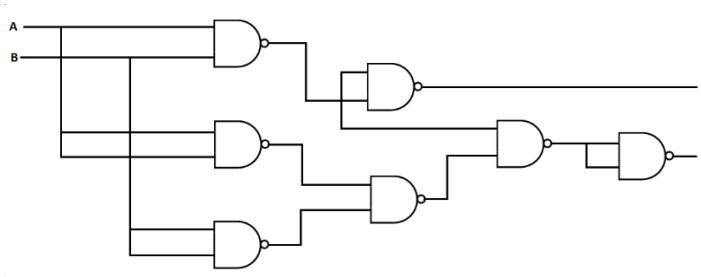
Pine Training Academy

Name Duration – 75 min

Mobile Number Question- 3 Marks each

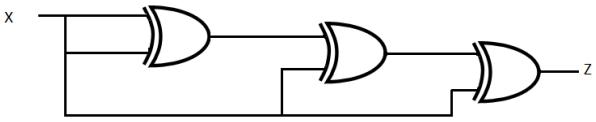
College Negative Marking -1

1. The time required for a pulse to change from 10 to 90 percent of its maximum value is called
   A. Rise Time
   B. Decay Time
   C. Propagation Time
   D. Operating Speed
2. The maximum frequency at which digital data can be applied to gate is called
   A. Operating Speed
   B. Propagation Speed
   C. Binary Level Transaction period
   D. Charging Time
3. What is the minimum number of two-input NAND gates used to perform the function of two input OR gate?
   A. One
   B. Two
   C. Three
   D. four
4. What logic function is performed by the circuit shown below?




   A. Ring counter
   B. Ripple Counter
   C. Full Adder
   D. Half Adder

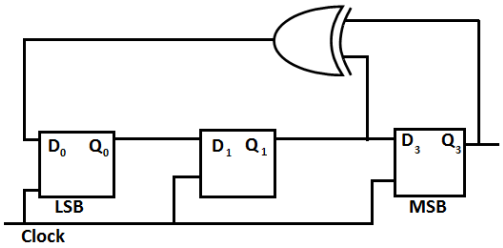
5. Output of the following circuit is




   A. 0
   B. 1
   C. X
   D. X’

6. What is the minimum number of 2 input NAND gates required to implement the function F = (x'+y') (z+w)
   A. 6
   B. 5
   C. 4
   D. 3

7. The correct state sequence of the circuit with initial state $Q_0$=1, $Q_1Q_2$ = 0. The state of the circuit is given by the value $4Q_2$+ 2 $Q_1$+$Q_0$




   A. 1,3,4,6,7,5,2
   B. 1,2,5,3,7,6,4
   C. 1,2,7,3,5,6,4
   D. 1,6,5,7,2,3,4

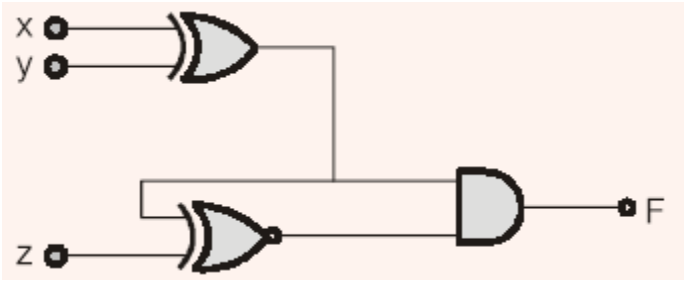
8. It is a counter where the flip-flops do not change states at exactly the same time, as they do not have a common clock pulse.
   A. Asynchronous Ripple Counter
   B. Synchronous Ripple Counter
   C. Counter
   D. All of above

9. In a combination circuit, each output depends entirely on the _____
   A. Same
   B. Different
   C. Common
   D. Immediate

10. A _____ circuit is not suitable in the synchronous circuit design because of its transparency nature.
   A. Latch
   B. Parallel
   C. Diagonal Circuit
   D. None of above

11. The characteristic equaton of any Flip flop describes the _____ of the next state in terms of the present state and inputs.
    A. Impact
    B. Behavior
    C. Path
    D. None of the above
12. Which table indicates the input condition of the flip flops necessary to cause all possible next state transitions of a flip-flop?
    A. Characterises table
    B. Truth Table
    C. Excitation Table
    D. Functional Table
13. When a circuit is self-correcting?
    A. If there are N-1 cycles among its unused states
    B. If there are N-1 cycles among its used states
    C. If there are no cycles among its used states
    D. If there are no cycles among its unused states
14. In this type of counter, the complement of the output of the last stage of the shift register is fed back to the D input of the first state.
    A. Ring counter
    B. Jhonson counter
    C. Straight Counter
    D. None of the above
15. Assuming 8 bits for data, 1 bit for parity, I start bit and 2 stop bits, the number of characters that 1200 BPS communication line can transmit is
    A. 10 CPS
    B. 120 CPS
    C. 12 CPS
    D. None of the above
16. Consider the representation of six-bit numbers by two's complement, one's complement, or by sign and magnitude: In which representation is there overflow from the addition of the integers 011000 and 011000?
    A. 2's complement only
    B. Sign and magnitude and 1's complement
    C. 2's complement and 1's complement
    D. All three representations

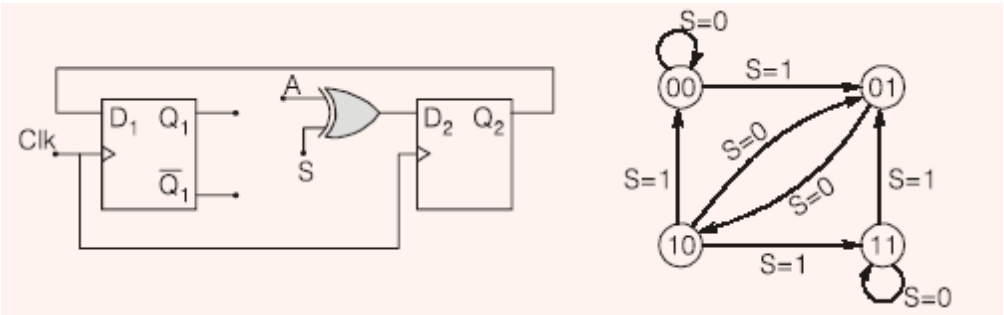
17. What is F




A. XY'Z + X'YZ
B. X'Y'Z + X'YZ'
C. X'Y'Z' + XYZ
D. XY'Z' + X'YZ'

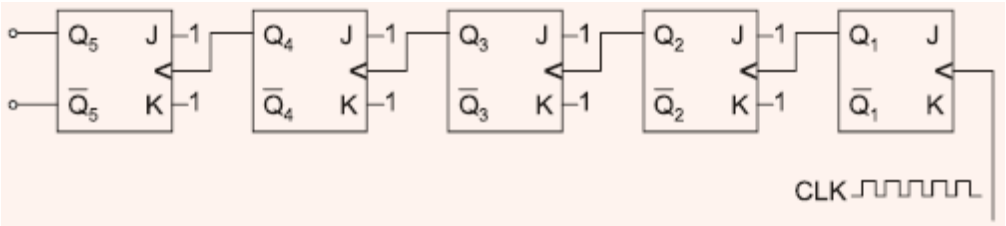
18. The following Boolean expression if F(w,x,y,z) = w'x'z' + wx'z' + xz + xy + w'y + wy. Then all the essential prime implicants of the expression
A. y, w'x'z', xy
B. xz, wy, wx'z'
C. y, xz, xy
D. y, x'z', xz

19. In the given circuit, if A is connected to Q1, the operation of the circuit is according to the state diagram. If XOR is replaced with XNOR, then to get the same operation of the circuit which of the following changes has to be done.



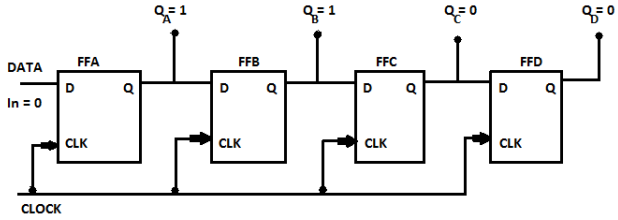

A. A should be connected to Q1'
B. A should be connected to Q2
C. A should be connected to Q1 and S is replaced by S'
D. A should be connected to Q1' and S is replaced by S'

20. The input frequency for the given counter is 1 Mhz. the output frequency observed at Q4 is _____.



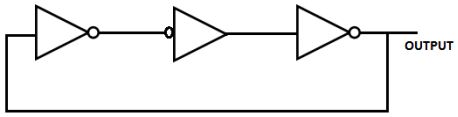

A. 62.5 kHz
B. 31.25 kHz
C. 1 MHz
D. Cannot determined

21. The logic circuit shown below operates as a




A. 4-bit asynchronous counter
B. 4-bit synchronous counter
C. BCD counter
D. SISO Shift Register

22. The circuit shown in the figure given below




A. Is an oscillator circuit and its output is square wave
B. Is one whose output remains stable in 1 state
C. Is one whose output remains stable in 0 state
D. Having a single pulse of 3 times propagation delay

23. The excess-3 code of decimal 7 is represented by
A. 1100
B. 0111
C. 1010
D. 1011

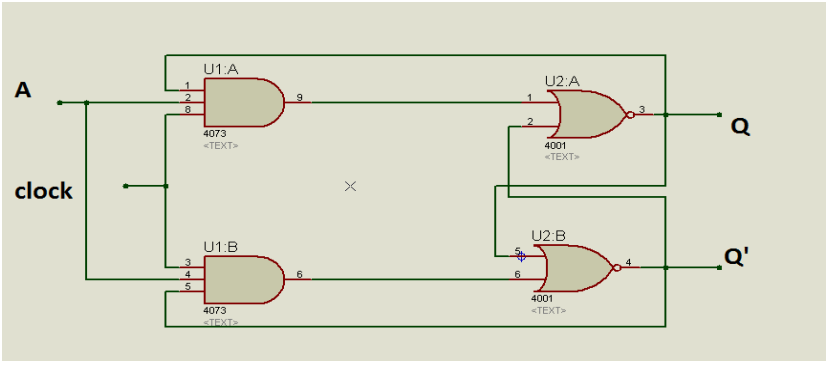
24. The logic 0 level of a CMOS logic device family is approximately
A. 1.2 V
B. 0.4 V
C. 5 V
D. 0 V

25. A eight stage ripple counter uses a flip-flop with propagation delay of 75 nanoseconds. The pulse width of the strobe is 50ns. The frequency of the input signal which can be used for proper operation of the counter is approximately
A. 1 MHz
B. 500 MHz
C. 2 MHz
D. 4 MHz

26. The conversation speed of an analog to digital converter is maximum with the following technique.
A. Dual Slope AD converter
B. Serial Comparator AD converter
C. Successive Approximation AD converter
D. Parallel comparator AD converter

27. How many address bits are required to represent 4K memory
    A. 5 bits
    B. 12 bits
    C. 8 bits
    D. 10 bits
28. DeMorgan's first theorem shows the equivalence of
    A. OR gate and XOR gate
    B. NOR gate and bubbled NAND gate
    C. NOR gate and NAND gate
    D. NAND gate and NOT gate
29. The access time of ROM using bipolar transistors is about
    A. 1 sec
    B. 1 msec
    C. 1 µsec
    D. 1 nsec
30. When signed numbers are used in binary arithmetic, then which one of the following notations would have unique representation for zero.
    A. Sign-magnitude
    B. 1's complement
    C. 2's complement
    D. 9's complement
31. In digital ICs, Schottky transistors are preferred over normal transistors because of their
    A. Lower Propagation Delay
    B. Higher Propagation Delay
    C. Lower Power Dissipation
    D. Higher Power Dissipation
32. A 4-bit synchronous counter uses flip-flops with propagation delay times of 15 ns each. The maximum possible time required for change of state will be
    A. 15 ns
    B. 30 ns
    C. 45 ns
    D. 60 ns
33. The hexadecimal number for $(95.5)_{10}$ is
    A. $(5F.8)_{16}$
    B. $(9A.B)_{16}$
    C. $(2E.F)_{16}$
    D. $(5A.4)_{16}$
34. Which of following requires refreshing?
    A. SRAM
    B. DRAM
    C. ROM
    D. EPROM
35. A weighted resistor digital to analog converter using N bits requires a total of
    A. N precision register
    B. 2N precision register
    C. N + 1 precision register
    D. N -1 precision register

36. Determine the analog output voltage of 6-bit DAC (R-2R ladder network) with Vref as 5V when the digital input is 011100.
    A. 2.1875 V
    B. 2.1870 V
    C. 2.1900 V
    D. 2.0000 V
37. What is conversion time of a Successive Approximation A/D converter which uses a 2 MHz clock and a 5-bit binary ladder containing 8V reference?
    A. 2.5 µS
    B. 1.2 µS
    C. 2.5 ms
    D. 1.2 ms
38. What is the Conversion Rate of above?
    A. 400000 conversions/sec
    B. 300000 conversion/sec
    C. 350000 conversion/sec
    D. Insufficient data to determined
39. A four-variable Boolean function, F , is expressed as (A, B, C and D are the logical variables): F = ∑ (0,1,2,5,8,9,10) The minimal product-of-sums expression for the Boolean function is
    A. (A'+B')(C'+D')(B'+D)
    B. (A+B)(B'+C+D)
    C. (A+C')(B+C)(A+D')
    D. (A'+D')(C'+B+D')
40. For the clocked flip-flop circuit shown below, what is the characteristics equation?

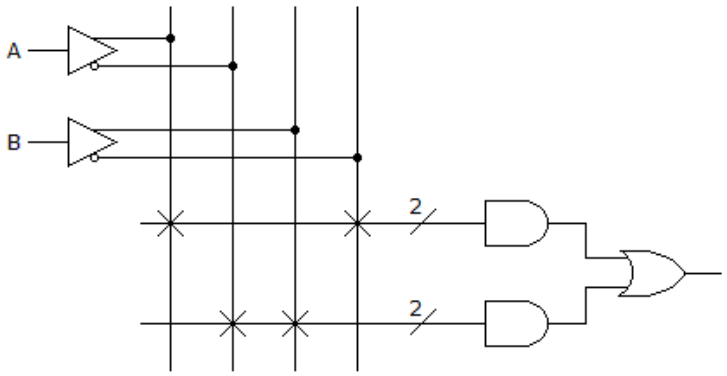



    A. Q(t+1) = AQ + A'Q'
    B. Q(t+1) = A'Q'
    C. Q(t+1) = AQ
    D. Q(t+1) = AQ'+A'Q
41. A basic multiplexer principle can be demonstrated through the use of a:
    A. single-pole relay
    B. DPDT switch
    C. Rotary switch
    D. Llinear stepper
42. The substraction of a binary number Y from another binary number X, done by adding the 2's Complement of Y to X, results in a binary number without overflow. This implies that the result is
    A. Negative and is in normal form
    B. Negative and is in 2's complement
    C. Positive and is in normal form
    D. Positive and is in 2's complement form

43. The output of a logic gate is '1' when all it's a input are at logic '0'. The gate is either
    A. A NAND or an E-OR gate
    B. A NOR or an EX-NOR gate
    C. An OR or an EX-NOR gate
    D. An AND or an EX-or gate
44. The _____ circuit overcomes the problem of switching caused by jitter on the inputs.
    A. Astable multivibrator
    B. Monostable multivibrator
    C. Bistable multivibrator
    D. Schmitt trigger
45. From the truth table below, determine the standard SOP expression

| Inputs | | | Output |
|---|---|---|---|
| A | B | C | X |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

    A. $X = \overline{A}\,\overline{B}\,\overline{C} + A\,B\,C + A\,\overline{B}\,C$
    B. $X = A\,B\,C + A\,B\,C + A\,B\,C$
    C. $X = A\,\overline{B}\,C + \overline{A}\,B\,C + A\,B\,\overline{C}$
    D. $X = \overline{A}\,\overline{B}\,C + \overline{A}\,B\,C + A\,B\,\overline{C}$
46. Which is the correct logic function for this PAL diagram?




    A. $X = \overline{A}\,\overline{B} + \overline{B}\,\overline{A}$
    B. $X = A\,\overline{B} + \overline{B}\,A$
    C. $X = A\,\overline{B} + B\,\overline{A}$
    D. $X = AB + BA$

47. For the following conditions on a 7485 magnitude comparator, what will be the state of each of the three outputs?

A0 = 0 B0 = 1 IA < B = 0

A1 = 1 B1 = 0 IA = B = 1

A2 = 1 B2 = 0 IA > B = 0

A3 = 0 B3 = 0

   A. A = B = 0, A < B = 0, A > B = 1
   B. A = B = 0, A < B = 1, A > B = 0
   C. A = B = 1, A < B = 0, A > B = 0
   D. A = B = 0, A < B = 0, A > B = 0

48. A ring counter consisting of five Flip-Flops will have
   A. 5 states
   B. 10 states
   C. 32 states
   D. Infinite states

49. The toggle condition in a master-slave J-K flip-flop means that Q and will switch to their _____state(s) at the _____.
   A. Opposite, active clock edge
   B. Inverted, positive clock edge
   C. Quiescent, negative clock edge
   D. Reset, synchronous clock edge

50. PALs tend to execute _____ logic.
   A. A.SAP
   B. B.SOP
   C. PLA
   D. SPD

| S. No | College | Board | Percentage/CGPA |
|---|---|---|---|
| | $10^{th}$ | | |
| | $12^{th}$ | | |
| | Diploma Final Year | | |
| | B.Tech $1^{st}$ Year | | |
| | B.Tech $2^{nd}$Year | | |
| | B.Tech $3^{rd}$ Year | | |
| | B.Tech $4^{th}$ Year | | |
| | M.Tech $1^{st}$ Year | | |
| | M.Tech $2^{nd}$ Year | | |



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