PINE TRAINING ACADEMY

Course Module

YOU'RE CARRIER, OUR PASSION

Summer Training Program on FPGA Logic System Design Using VERILOG.

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Pine Training Academy

4/18/2014

Summer Training Program on FPGA Logic System Design using VHDL.		
Module	**Detailed Syllabus**	**Duration**
Module1 Introduction.	• Introduction to Pine Training Academy. • Introduction of Semiconductor Industry. • Introduction of VLSI- ASIC & FPGA FLOW. • Study/Revision of Digital System Design. • Schematics Entry – Practical on ISE/VIVADO.	Week 1.
Module 2 FPGA/CPLD: - FPGA Device and FPGA Design Flow.	• XILINX FPGA and CPLD Introduction. • Feature. • Architecture. • Packaging. • CLB Overview. ➢ SLICE ➢ LOGIC Cell ➢ LUT ➢ Carry and Control Logic. • IOB. • RAM BLOCK. • Multiplier. • Memory. • DCM. • FPGA Nomenclature. • Written test on Module 2. • Project Assignment and Project Study: - Industrial Project uses Verilog and Implementation on FPGA.	Week 1.
Module 3 HDL- Verilog and Simulation Lab.	• **Introduction :-** ➢ The scope and application of Verilog. ➢ Design and tool flow. ➢ Types of compilation, Simulation and Synthesis on FPGAs. • **Module:-** ➢ Structure of basic Verilog program. ➢ Basic elements of Verilog:-Defining Modules: ports lists, port modes, parameters, Instance type.	Week 2, 3 and 4.

- **Language Elements:-**
  - Identifiers, Comments, Compiler Directives.
  - Value Set: integers, real's, strings.
  - Data Type: net, vectored, scalar and registers.
- **Expressions:-**
  - Arithmetic operator.
  - Logical operator.
  - Relational operators.
  - Miscellaneous operators.
- **Modelling:-**
  - Gate Level Modelling.
  - UDP.
  - Data Flow Modelling.
  - Behavioural Modelling:- Procedural Constructs, Timing Controls, Block Statement, Procedural assignment, conditional statement, loop, cases, procedural continuous assignment.
  - Structural Modelling
- **Example Designs:-**
  - Combinational Design.
  - Sequential Design.
- **FSM Synthesis :-**
  - Verilog coding styles for FSMs.
  - State encoding, Unreachable states and input hazards.
- **Memories:-**
  - Array types.
  - Modelling memories.
  - Implementing ROMs & RAMs.
- **Advanced Verilog:-**
  - System Task.
  - Function.
  - Test benches.
  - verification
- Industrial Project:-Discussion of project start from 1st week and daily 1 hr. discussion on project with student.
- Written Test on HDL-VHDL.
- Project Work (Continue in every week).

Module 4
FPGA Design Flow and Study of FPGA Development board.
	• **Synthesis**.
	  ➢ Pre- Synthesis Simulation.
	  ➢ Post Synthesis Simulation.
	  ➢ Synthesis Technique.
	  ➢ Analysis of Report.
	• **PlanAhead- ISE**.
	  ➢ UCF.
	• **Implementation.**
	  ➢ Translation.
	  o Post Translation Simulation.
	  ➢ Mapping.
	  o Post Mapping Simulation.
	  ➢ Placement and Routing.
	  o Post Placement and Routing Simulation.
	  ➢ Implementation Technique and Analysis of Report at each stage.
	• **Programing**.
	  ➢ FPGA Programming.
	  ➢ FLASH Programming.
	• Project work Continue.
	• Written test on Module 4.
		Week 5.

Module 5.
Development Board- Xilinx.
	• Study of Xilinx Spartan 6 SP605 /SP601 Development Board.
	  ➢ Study of Interface.
	  o LED.
	  o Switch.
	  o Button.
	  o DIP.
	  o FLASH.
	  o UART.
	• Completion of Project, Viva and Hanover of Certificate.
		Week 6.

Batch Start: 2nd week of June, 2014.

Batch Size: 20 seats.

Duration: 4-6 week, 6-8 hrs. Per day***.

Eligibility Criteria:

1. B.E. or B. Tech with Average 60 % from E & C, E & I, E & E, Computer Science .

Perquisite:-

1. Knowledge of Advanced and Basic Digital System.

Required:-

LAPTOP: – With Minimum Configuration DUAL CORE or i3 or i5 Processor, 2/4 GB DDR3, 500 HDD with window XP or Window 7.

FEES and Payment Schedule Details:
Course Fees: Rs 5000 +12.36 % Service Tax.
Registration Fees: Rs 500.

Mode of Payment- Through Cheque or Cash.

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