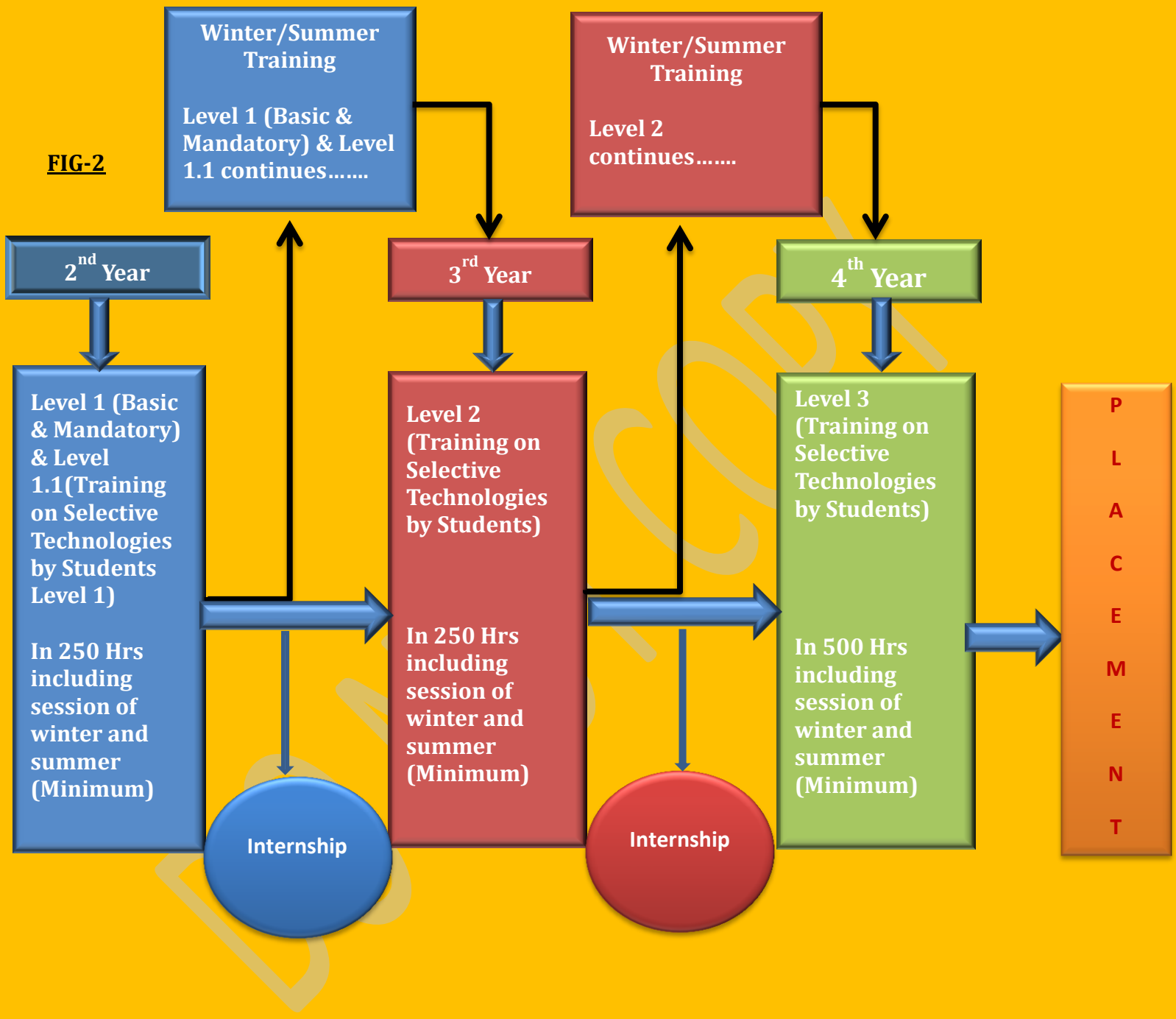
Method We follow- How to Get Entry Pass in SEMICODUCTOR Industries for 2nd year engineering students

FIG-2



FPGA System Design

Course Structure for 2nd year

Analog (10 Hrs)- Module 1	Digital (20 Hrs) Module 2	Programing (50 Hrs) Module 3 - RTL	FPGA (10 Hrs) Module -4
• Diode • BJT • Fabrication Process	**Digital Electronics** • **Boolean Algebra** • **Karnaugh Map** • **Logic Gates** • **Numbers system** • **Combinational Circuits** • **Sequential Circuits** • **FSM** • **Tutorial** • **HANDS ON (All gates, combinational and sequential circuit's simulation on Xilinx ISE Design and Vivado Design Suite).** • **Project using Schematics – CRC, Parity Checker, Boot Multiplier, FIFO and Memory etc.**	**Verilog** • **Introduction Module** • **Data Types and test Bench** • **Data Flow and Test Bench.** • **Gate level and Test Bench.** • **Procedural Blocks and Test Bench.** • **Language Operator** • **Coding Technique.** • **Synthesis wrt to coding.** • **Optimization wrt to coding.** • **Hands on Synthesizable coding technique.** • **Project – Simulation based project like FIFO etc. and HW based Project like Display and LED control on XILINX Artix 7 board.**	**Module D-10 Hours-FPGA** • **CLB architecture.** • **LUT architecture.** • **Slices.** • **Wide Multiplexer.** • **I/O Bank Structure.** • **Clock Managers.** • **CMT/PLL (Virtex 6).** • **Block RAM Memories.** • **DSP Slices.** • **Working on FPGA Spartan 6 and Artix 7 Development board with real time project.**

FPGA System Design

Course Structure for 3rd year

Digital – Advanced (20 Hrs) Module 5	HDL- VHDL – (50 Hrs) Module -6 - RTL	FPGA Implementation (20 Hrs) Module -7	Analog (10 Hrs) Module -8
• Advanced Digital Topic wrt to written test and Interview. FSM Counter Register FIFO • Timing Fundamental (STA) • Working on Linux Environment. • Scripting - TCL	VHDL Course Outline • Entity/Architecture • Logical Operators • Data Types • Concurrent • Sequential Statements • Relational operators • Process, IF THEN WHEN ,CASE, Signals • Describing Clocks • Introducing IEEE 1164 STD_LOGIC • Counter designs • Entity Modes • Making FSM Coding • Enumerated Types • State Machine design Methods • State Machine encoding • Hierarchy • Using PORT MAP to construct design • Package, Function, Configuration. • Using Black Boxes • GERNERICs • Process variables • Process Loops • Generate Statements • Synthesizable coding technique. • The Test Bench • Project both SW and HW implementation on FPGA Boards.	• Real Time Simulation – Chipscope. • Design using Xilinx Coregen and Vivado IP Integrator. • Timing Analysis using Timing concept on XILINX Tools wrt to timing failure in design. • Working on FPGA Tools feature wrt to Synthesis and Implementation strategies. • FLASH Programing. • Tools Used – XILINX ISE/VIVADO • Modelsim • Altera – Quartus	• MOSFET Fundamental • Fabrication Process. • Analog Fundamental • CMOS Inverter Fundamental • Differential Amplifier

FPGA System Design

Course Structure for 4th year

FPGA Embedded Design (75 Hrs) Module-9	DSP FPGA Design (75 Hrs) Module 10	DSP FPGA Continue	Industry Standard Project based on expertizes.
• Introduction to Embedded System. • Introduction to FPGA based Embedded System. • Embedded Support on FPGA. • Processor C for FPGA. • Embedded Processor – RISC 32 Bit. • ZYNQ Architecture. • XILINX Tools for Embedded Design. • Introduction to Embedded Linux. • Embedded Linux Porting Concept. • Embedded Linux on ZYNQ. • Working on FPGA/ZYNQ.	• Introduction of Matlab and Simulink. • FPGAs for DSP. • Introduction to System Generator. • Simulink Basics. • Arithmetic Operations. • Fixed Point Format- Signed and Unsigned (with or without binary point). • Gateway In & Out. • Saturation and Wrap in fixed point numbers. • Applications of Round and Truncate in fixed point while arithmetic operations. • Hardware Cost of Saturation, Wrap, Round and Truncation. • Addition, Subtraction, Multiplication, Division, Scaling and Shifting. • Complex arithmetic- Complex multiplication, conjugate etc. • Library Overview • Use of blocks available inside Xilinx Block sets' Library- Basic blocks. • Handshaking blocks- FIFO, BLOCK RAM etc. • Signal Processing Blocks- FFT, FIR etc. • Data storing blocks- ROM. • Black Box- HDL import. • CORDIC • Arithmetic Functions in	• Phase Truncation techniques. • Sine wave generation using DDS Compiler. • Applications. • INTRODUCTION TO ANALOG AND DIGITAL COMMUNICATION. • Analog modulation schemes. • Analog Transmitter- AM-SSB/AM-DSB/FM. • Analog Receiver- AM-SSB/AM-DSB/FM. • Basic Modulation Schemes like PSK, FSK, QAM, OFDM etc. • PSK based Modulator. • Pulse Shaping and Matched Filtering and its implementation. • PSK based Demodulator. • Communication Link. • Channels and Channel Equalization. • Eb/No Vs BER plots for PSK schemes. • DUC & DDC DESIGN IN SYSTEM GENERATOR. • Digital up	• Project on Embedded System Design on FPGA. • Project on DSP System Design on FPGA. • Project on RTL (Only one Project Applicable)

	Circular Co-ordinates. • Implementations. • CORDIC Complier. • FIR & IIR Filtering • Sampling, Sub-Sampling, NY Quist-Criterion, Mixing, Quadrature Modulator &I-Q. • Single Rate and Multi-Rate Filters, MAC filters. • Interpolation & Decimation. • Difference between Up sampling, Interpolation. • Half- Band Filters and its implementation. • Interpolation FIR filter and its implementation using FDA Tool. • Decimation FIR Filter-with various windowing techniques and its implementation using FDA Tool. • Poly-Phase Filters. • IIR Filter and its implementation using FDA Tool. • Effects of Quantization • LOW PASS CASCADED INTEGRATED COMB (CIC) FILTERS. • Brief Overview of Decimation and Interpolation. • CIC Filters Theory and its Construction. • Interpolation and Decimation with CIC. • CIC Compiler. • Compensation FIR • NUMERICALLY CONTROLLED OSCILLATOR (NCO). • Look Up Table Technique.	Convertors and Digital down Convertors. • Implementation Using either FIR filters or CIC filters, • SNR improvement in DDC. • DUC & DDC DESIGN IN SYSTEM GENERATOR. • Digital up Convertors and Digital down Convertors. • Implementation Using either FIR filters or CIC filters, • SNR improvement in DDC. • HARDWARE CO-SIM & USE OF CHIPSCOPE ANALYZER. • Analyze Design using Timing and Power Report. • Creating HDL. • Creating NGC. • Creating Bit stream. • Analyze Complete Design using CHIPSCOPE ANALYZER. • Hardware Co-Simulations.	

PCB (Board) Design

Course Structure for 2nd year only

BASIC ANALOG – Module 1	BASIC DIGITAL- Module-2	CIRCUIT SIMULATION- Module-3	BASIC OF PCB DESIGN- Module -4
➢ Resister. ➢ Capacitor. ➢ Inductor ➢ Diode. ➢ Led. ➢ Basics of circuit design.	➢ Transformer. ➢ 7805. ➢ 7812 ➢ Lm317. ➢ All logic gates and their IC.	➢ Circuit simulation on bread board. ➢ Circuit simulation on proteus. ➢ Introduction of PCB designing.	➢ Introduction of EAGLE (tool for PCB designing.) ➢ Introduction of schematic design. ➢ Introduction to selecting component from library. ➢ Introduction to board design.