PINE TRAINING ACADEMY

Course Module

YOUR CAREER, OUR PASSION

Certified Online Course in ASIC Verification.

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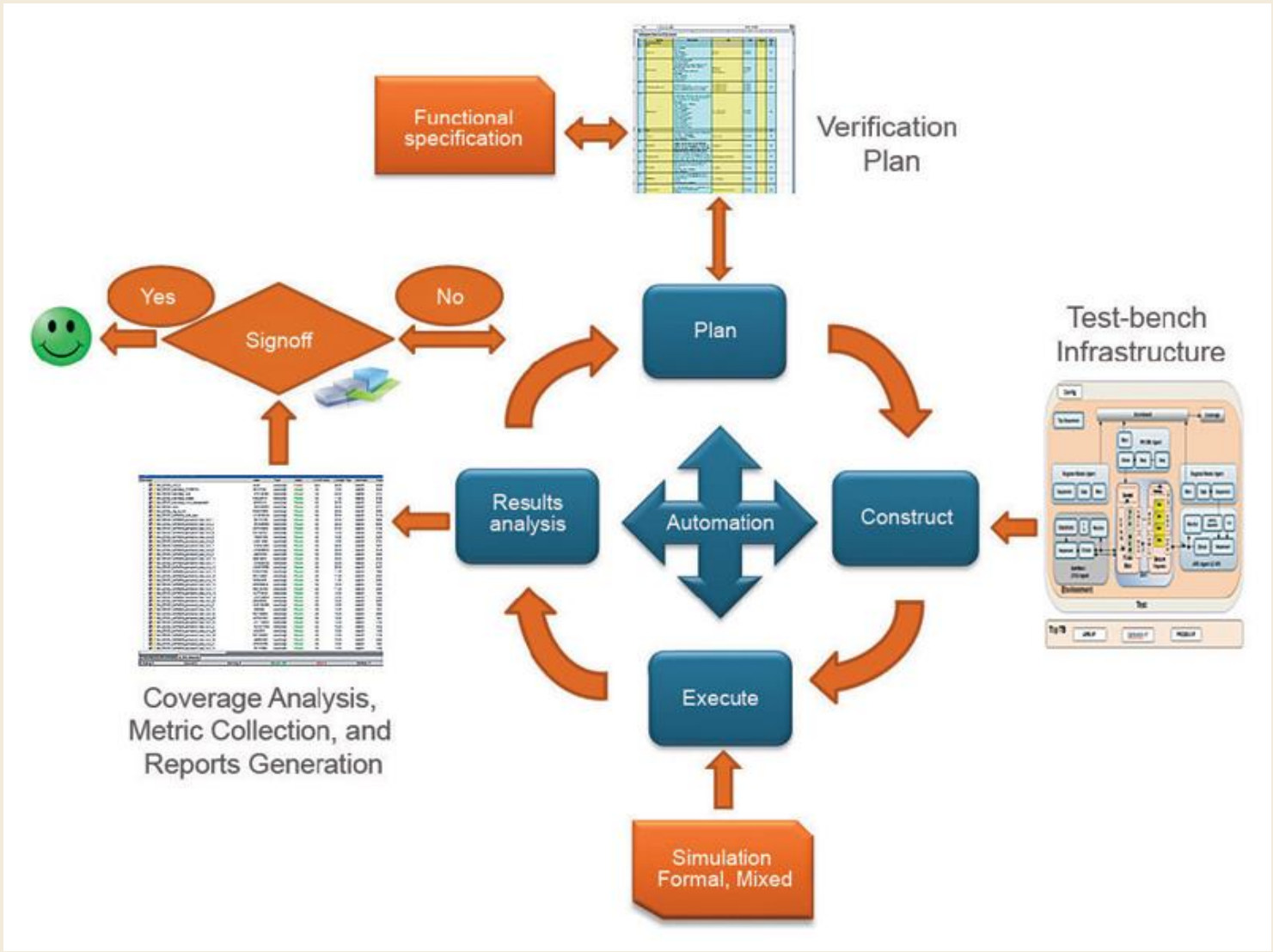
Pine Training Academy

Verification Flow in Design Signoff



Highlights

- Understanding of Black box verification and White box verification
- Understanding of different verification (IP Verification, SoC Verification, Subsystem Verification, Verification IP Design)
- Digital Logic Fundamental like Basic and Advanced Digital.
- Brief Study of C and Object Oriented programming.
- Basic knowledge of Linux and Scripting.
- Hardware Design Language (Verilog).
- Hardware Verification Language (System Verilog)
- Verification Methodology (UVM)
- Brief study of AMBA Bus (APB,AHB,AXI).
- Industrial Project.
- Test and Interview Series after completion of every module.
- Visit from Industry.
- Personality Development program and preparation of Interview and Resume.

	ASIC Verification		
Main Module	**Digital System Design**		

Module -1 Digital System Design.	❖ Digital System Design:-
	• Introduction to Digital System.
	  ○ Number System
	  ○ Digital Logic Levels
	• Digital Logic Circuits.
	  ○ Combinational Logic Circuit.
	  ○ Sequential Logic Circuit.
	• Schematics Entry.
	• FSM.
	• Timing Fundamental.
	• Assignment of Industrial Project.
	• Test and Interview Series.		

Module – 2 UNIX	❖ UNIX • Basic of UNIX, how different from Windows. • Introduction of SHELL. • File and Directories. • Home Directories Introduction and .cshrc file formation. • Basic Commands-cp,mv,rm,touch,which, mkdir,cat • UNIX sed , cut ,awk,grep (regex),tr commands. • BASH shell scripting, usage of loops, arguments, array.		
Module – 3 C, OOP concept	❖ C & Object Oriented Programming • C and Verification • Why C is useful in Verification • Complete C programming language brief • Object oriented programming and Verification • Brief of Object Oriented Programming		
Module -4 HDL(Hardware Design Language)	❖ Hardware Design Language (Verilog). • Need of Verilog • Abstraction Level • Concurrency • Digital Circuit design with Verilog • Need of Verification of HDL design • 4 State & 2 State logic • Top Down & Bottom up design Methodology • Verilog HDL Design Flow		

	• Verilog Syntax and Semantics • Gate level Modelling • Data Flow Modelling • Behavioural Level Modelling • Blocking & Non-blocking assignment • Test & Interview questions		
Module – 5 System Verilog(HVL)	❖ **Introduction to System Verilog course objective.** • Introduction: Reasons for using the Hardware Verification Language. • Benefits of System Verilog in Verification. • System Verilog Data types • Procedural Statements and Routines • Interface & Virtual Interface • Constraint Randomization & Need of Randomization • Threads & Interprocess Communication • Coverage Metric(Code coverage, Functional Coverage) • Callbacks • Cross coverage ❖ Writing a Test – bench. ❖ Test and Interview Series.		
Module– 6 UVM Methodology	❖ Universal Verification Methodology(UVM) • UVM Testbench • UVM Phases • UVM Top-down & Bottom-up approach • UVM Reporting • UVM Transaction • UVM Configuration • UVM Factory • UVM Sequence (also UVM Virtual sequence) • UVM Components(Monitor, Agent, Environment , Sequencer, Driver) • UVM Transaction level Methodology • UVM Callbacks		

Module -7 AMBA Bus	❖ Advance Microcontroller Bus Architecture ❖ APB ❖ AHB ❖ AXI ❖ Why AMBA is so important for Verification? ❖ One Project of Verification IP development for any AMBA bus.		
Module – 8 TCL	❖ TCL :The command and topics covered in Tcl are • Set • Puts • String cmd & its various options 3.1 compare 3.2 equal 3.3 first 3.4 last 3.5 index 3.6 is class 3.7 length 3.8 map 3.9 match 3.10 range 3.11 repeat 3.12 replace 3.13 reverse 3.14 tolower 3.15 toupper 3.16 totitle 3.17 trim 3.18 trimleft 3.19 trimright 3.20 wordstart 3.12 wordend • List and its various options 4.1 lappend 4.2 lindex 4.3 linsert 4.4 llength 4.5 lmap 4.6 lrange		

	4.7 lrepeat 4.8 lreplace 4.9 lreverse 4.10 lsearch 4.11 lset 4.12 lsort • Concat • Format • Scan • Glob • Global • Incr • Expr • Join • Split • foreach loop • If loop • for loop • switch • while loop • catch • clock • regexp • regsub • Tcl procedures- return,non return, args,optional arguments etc. • file handling:- open & close • file command and its various options • argc,argv,argv0 • arrays • upvar • after • Namespaces • Source • Unset • Exec • Exit • Flush • Time • Break • Continue		

	• Read ❖ Test and Interview.		