	Physical Design
Main Module	
Module – 1 UNIX	❖ UNIX • Basics of UNIX, how different from Windows. • File and Directories. • Home Directories Introduction and .cshrc file formation. • Basic Commands-cp,mv,rm,touch,which, mkdir,cat • UNIX sed, cut, awk, grep (regex),tr commands. • BASH shell scripting, usage of loops, arguments, array. • Test and Interview Series
Module -2 Introduction of IC Design Flow	❖ Understanding of ASIC design flow and it's all stages along with inputs and outputs and all checks. ❖ Understanding of FPGA Vs ASIC design flow. ❖ Test and Interview Series
Module – 3 CMOS fundamentals	❖ Introduction of MOSFET and its functioning. ❖ Basic principle and characteristics of CMOS ❖ Implementations of digital circuits using CMOS. ❖ Different types of Basics gates used in ASIC design. ❖ Test and Interview Series.
Module– 4 Data Types & Flow Basics	❖ Understanding of different data types ○ LEF ○ Libs ○ DEF ○ SPEF ○ Netlist ○ SDC ❖ Different types of PVT conditions ❖ Understanding of Netlist to GDS flow ○ Floor planning ○ Power planning ○ Placement ○ CTS ○ Routing ❖ Test and Interview Series

Module -5 Floorplanning **Power Planning**	1. What is floorplanning 2. Objective of floorplaning 3. Inputs and outputs of floorplanning 4. What is core and die. 5. Die size estimation, design utilization and aspect Ratio. 6. IO placement 7. Macro Placement 8. Different types of Physical cells 9. Different types of Blockages 10. Channel estimation between two macros. 11. Challenges of floorplanning 12. What is power analysis 13. IR and EM analysis 14. P/G grid distribution 15. Why worry about voltage drop ❖ Test and Interview Series
Module – 6 Placement	❖ What and why placement ❖ Goals of Placement ❖ What is standard cells ❖ Types of placement strategies ❖ Placement optimization techniques ❖ Understanding of timing constraints ❖ Cell and nets delay calculation ❖ Congestion and how to analyse and deal with it ❖ Different types of Vt cells ❖ Real Design Placement challenges ❖ Test and Interview.
Module – 7 Clock Tree Synthesis	❖ What is CTS and why we need it ❖ Goal of CTS ❖ Input and output of CTS stage ❖ Different terminologies of CTS like , ○ Skew ○ Clock latency and network latency ○ Clock transition ○ clock jitter ○ clock uncertainty ❖ CTS constraints and specifications

	❖ CTS strategies and techniques ❖ Understanding of CCOPT ❖ CTS challenges ❖ Test and Interview.
Module – 8 Routing	❖ What is Routing and why should we need it. ❖ Goals of Routing ❖ Input and output of routing stage ❖ HVH and VHV models ❖ Routing operations o Global Routing o Track Assignment o Detail Routing o Search and Repair ❖ Routing challenges ❖ Types of DRC and how to clean it ❖ Test and Interview.
Module -9 STA fundamentals	❖ What is STA and why we need to do STA in the flow ❖ Different types of STA terminologies ❖ What is Setup and Hold time ❖ Setup and hold time calculation with examples ❖ Different techniques used to fix setup and hold issue in the different stages. ❖ Test and Interview Series
Module -10 Signoff	❖ Different types of physical verification check including o DRC check o LVS check o Antenna check o CDM check o ERC checks o DRC checks o Timing closure ❖ RC extraction ❖ ECO ❖ Test and Interview Series